



WBS 3.1 - Trigger

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CMS Trigger Project Manager

DOE/NSF Review
June 5, 2002

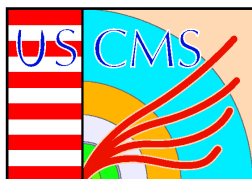
This talk is available on:

http://hep.wisc.edu/wsmith/cms/Trig_Lehman_Plen02.pdf

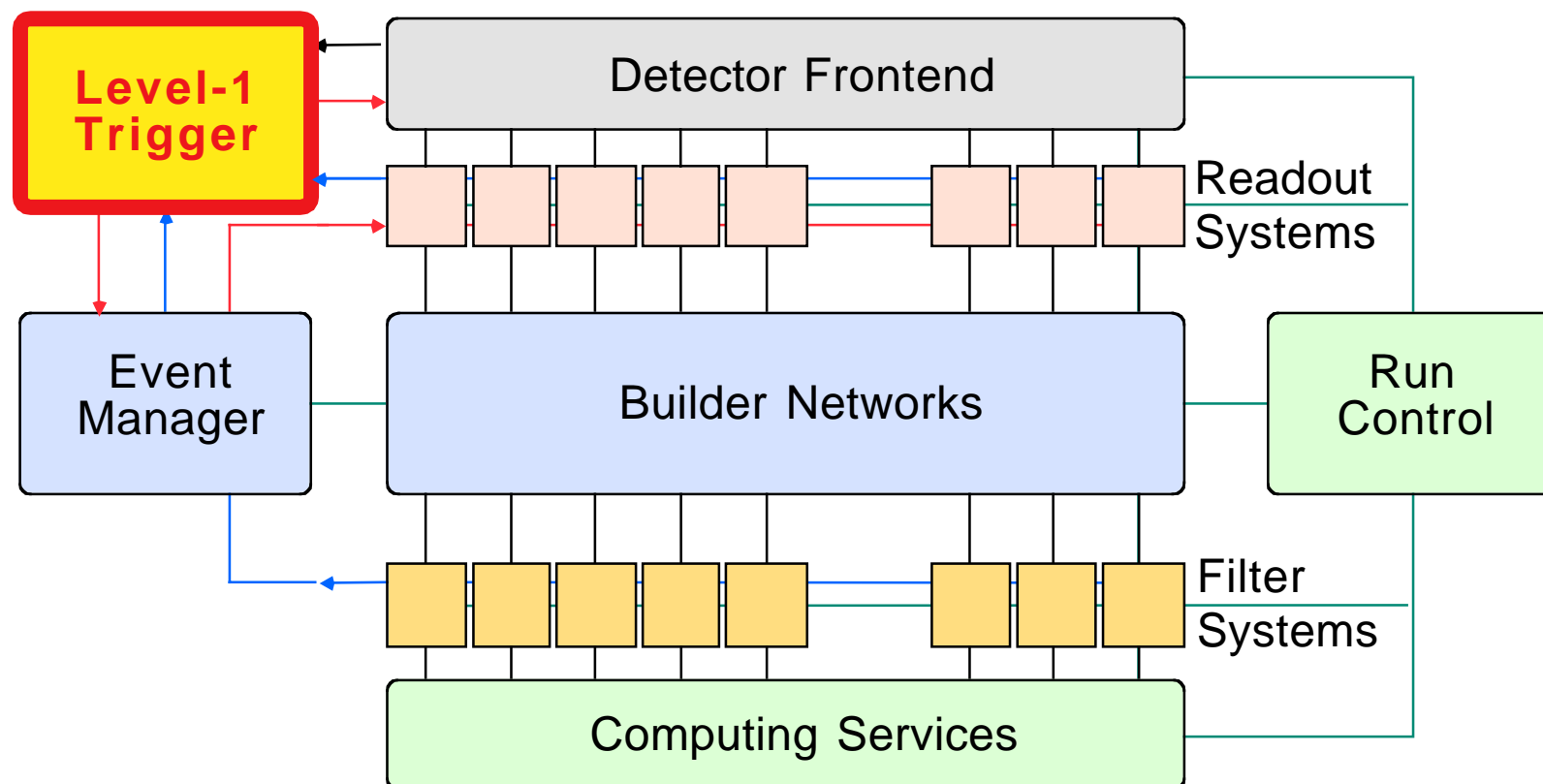


Outline

- **Overview of Calorimeter Trigger**
- **Calorimeter Trigger Status & Plans**
- **Overview of Muon Trigger**
- **Muon Trigger Status & Plans**
- **Cost and Schedule Performance**
- **Concerns**
- **Summary and Conclusions**

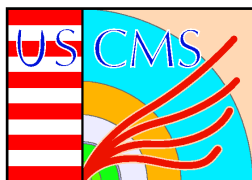


Trigger & DAQ Systems



Level-1 Trigger Requirements:

- Input: 10^9 events/sec at 40 MHz at full $\mathcal{L} = 10^{34}$
- Output: 100 kHz (50 kHz for initial running)
- Latency: 3 μ sec for collection, decision, propagation

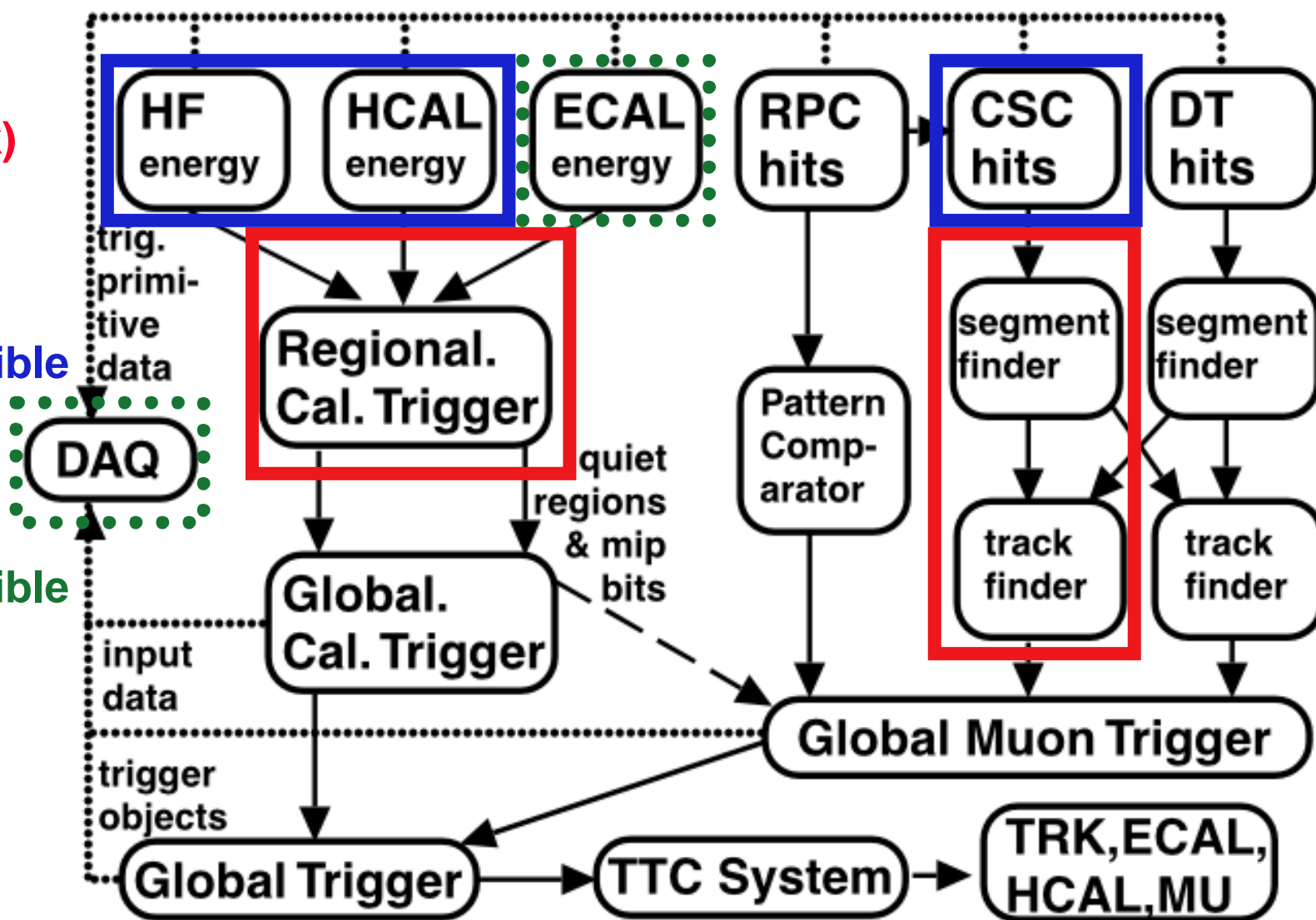


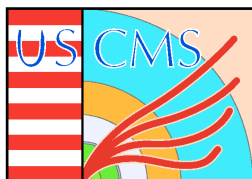
L1 Trigger Hardware Overview

US CMS
Trigger
(this talk)

US CMS
fully
responsible

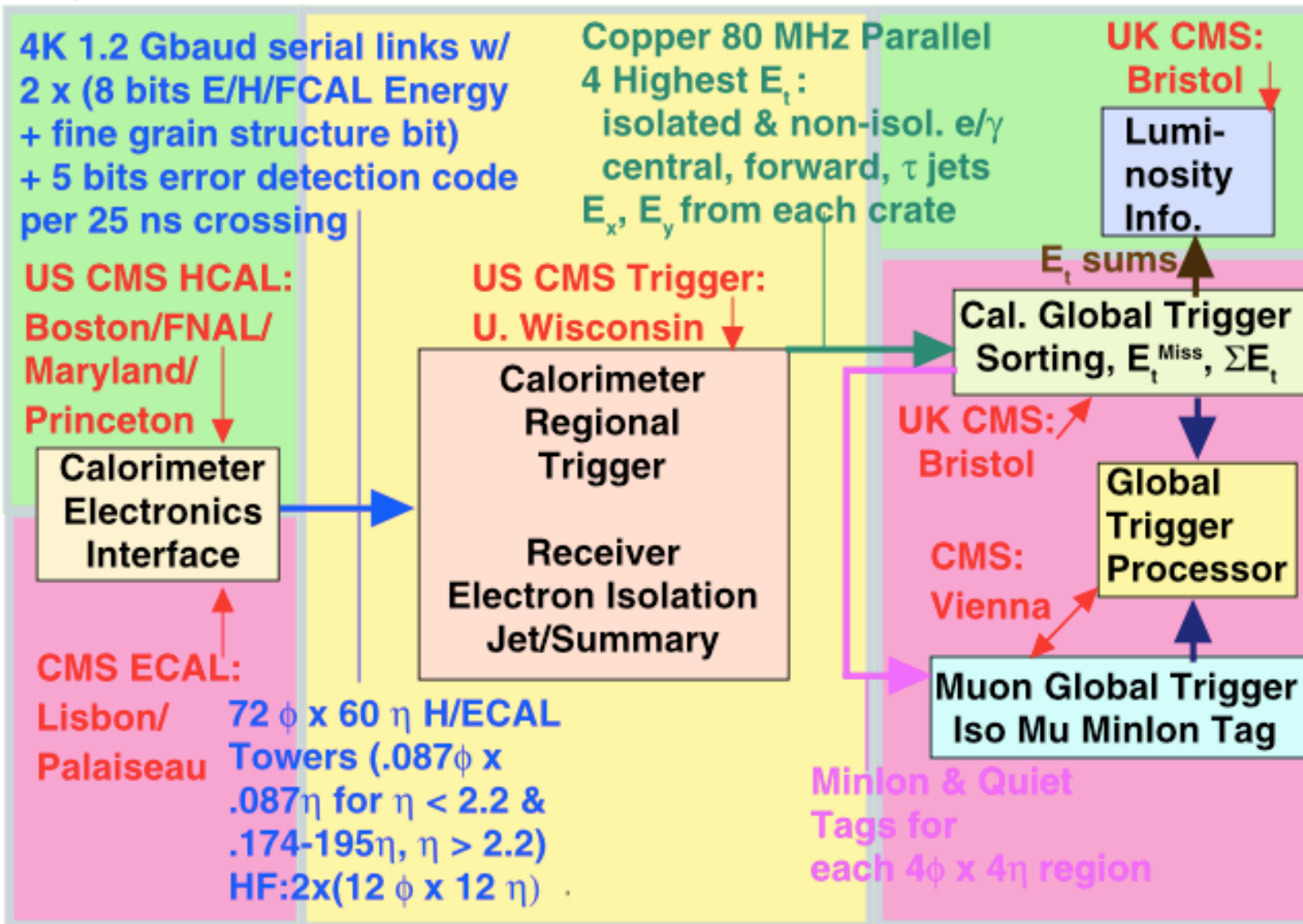
US CMS
partially
responsible

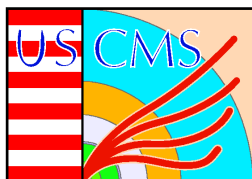




Calorimeter Trig. Overview

(all located in underground counting room)

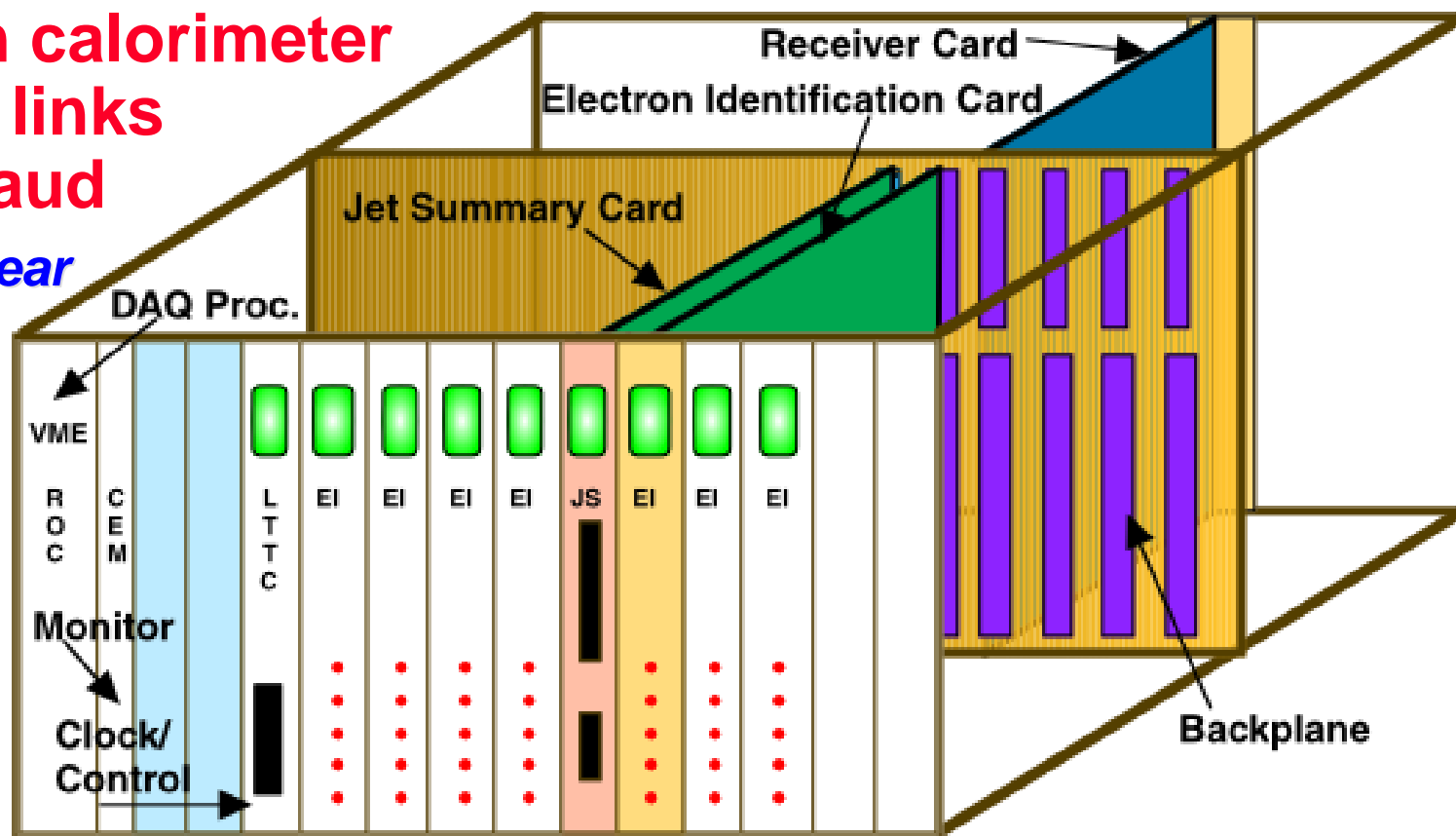




Calorimeter Trigger Crate

Data from calorimeter
FE on Cu links
@ 1.2 Gbaud

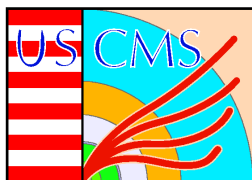
- Into 126* rear Receiver Cards
- Prototype tested w/ ASICs



160 MHz point to point backplane (proto. tstd.)

- 18 Clock&Control (proto. tstd.), 126 Electron ID (proto. tstd.), 18 Jet/Summary Cards -- all cards operate @ 160 MHz
- Use 5 Custom Gate-Array 160 MHz GaAs Vitesse Digital ASICs
 - Phase, Adder, Boundary Scan, Electron Isolation, Sort (manufactured)

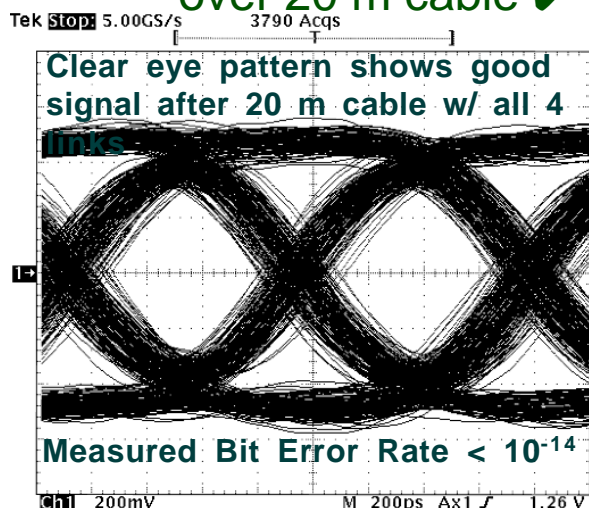
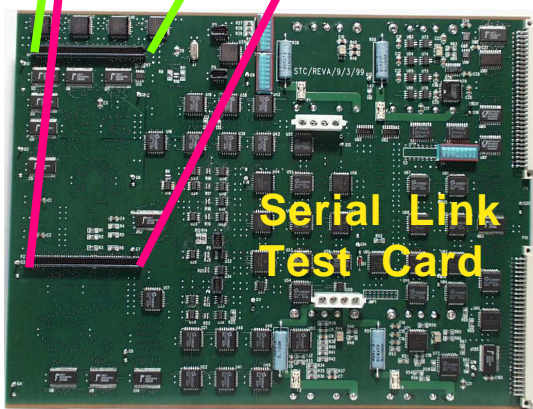
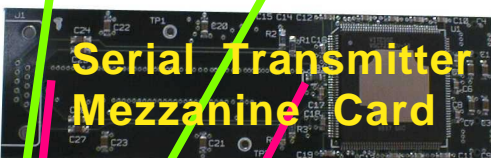
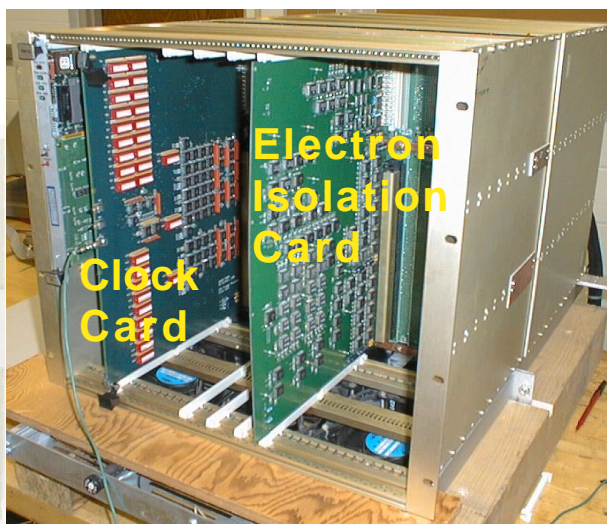
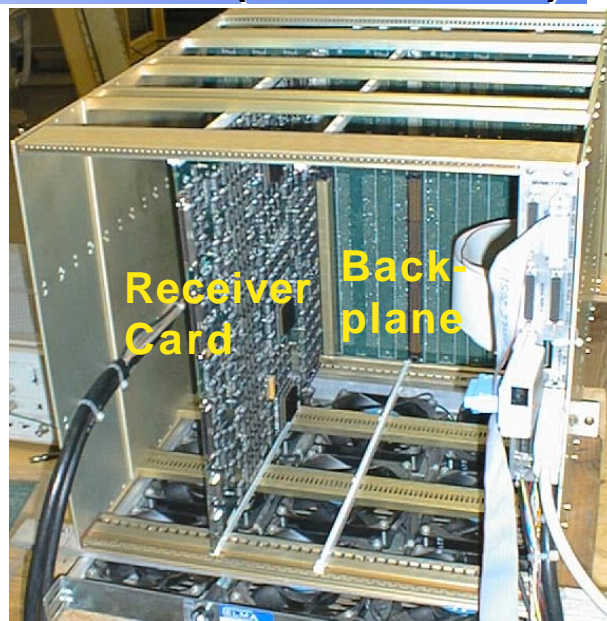
Spares not included*



1st Generation Calorimeter Trigger Prototype Tests (U. Wisconsin)

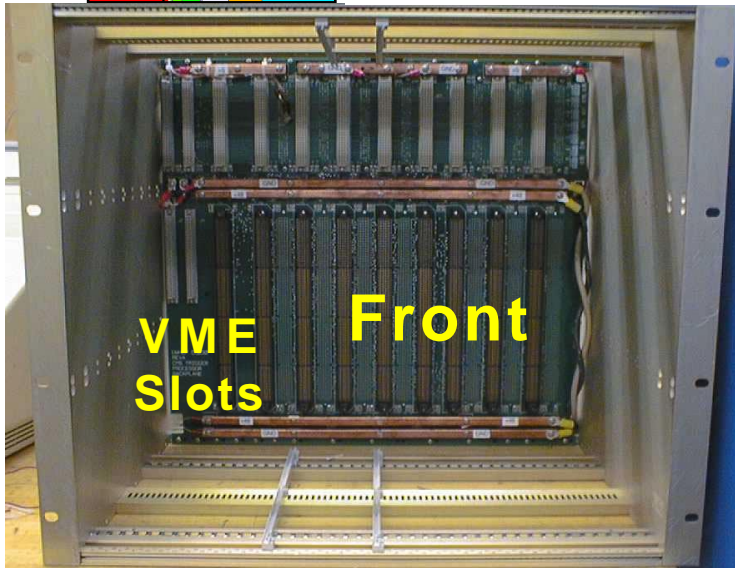
Successful Prototyping Program

- Crate & 160 MHz Backplane tested ✓
- Clock Card tested ✓
- Receiver Card tested (w/ Adder ASIC) ✓
- Adder ASIC tested & production finished ✓
- Electron Isolation Card tested ✓
- 4 x 1.2 Gbaud Copper Serial Link system:
 - Successfully transmits data at 4 Gbit/s over 20 m cable ✓

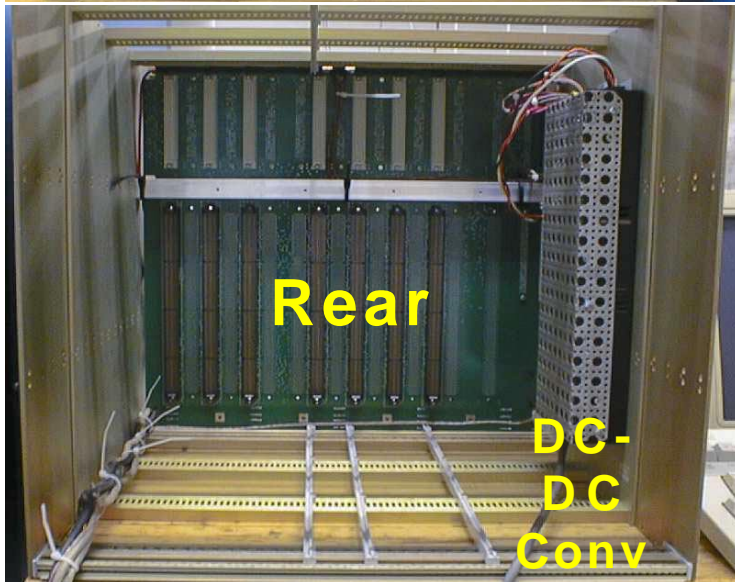




Cal. Trig. 2nd Gen. Prototypes (U. Wisconsin)



VME Slots Front



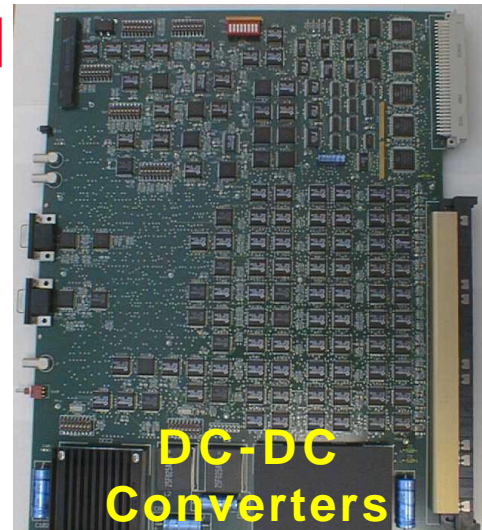
Rear DC-DC Conv

New High-Speed Backplane

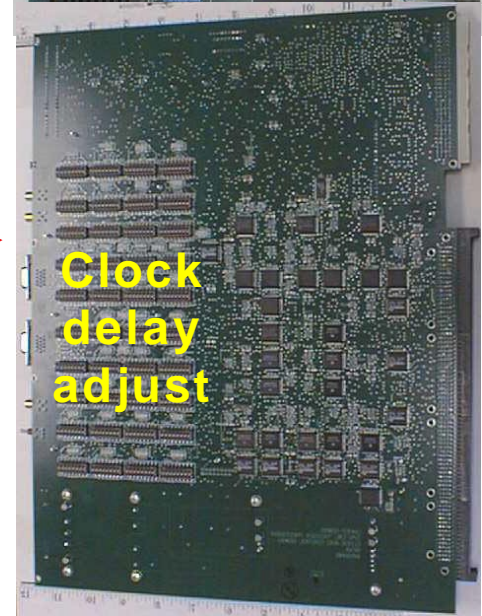
- 160 MHz with 0.4 Tbit/sec dataflow
- Mostly tested
- Designed to incorporate algorithm changes
- New Non-Isolated Electron, Tau & Jet Triggers

New Clock & Control Card

- Fans out 160 MHz clock & adjusts phases for all boards
- 50% tested



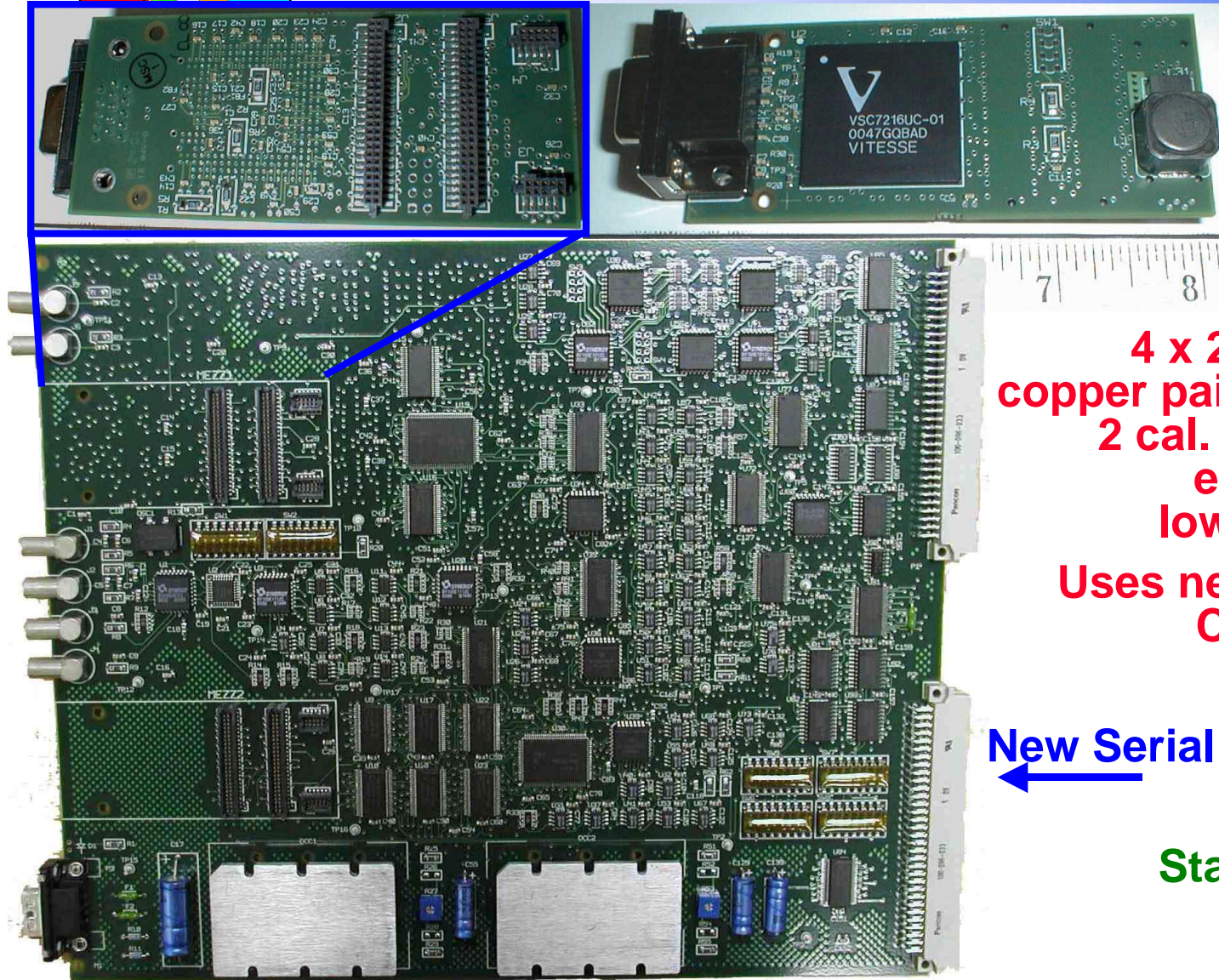
DC-DC Converters



Clock delay adjust



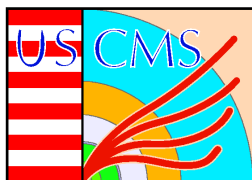
New Cal. Trig. 4 Gbaud Copper Link Cards & Tester (U. Wisconsin)



8 Compact Mezzanine Cards for each Receiver Card accept 4 x 20 m 1.2-Gbaud copper pairs transmitting 2 cal. tower energies every 25 ns with low cost & power. Uses new Vitesse Link Chips (7216-01).

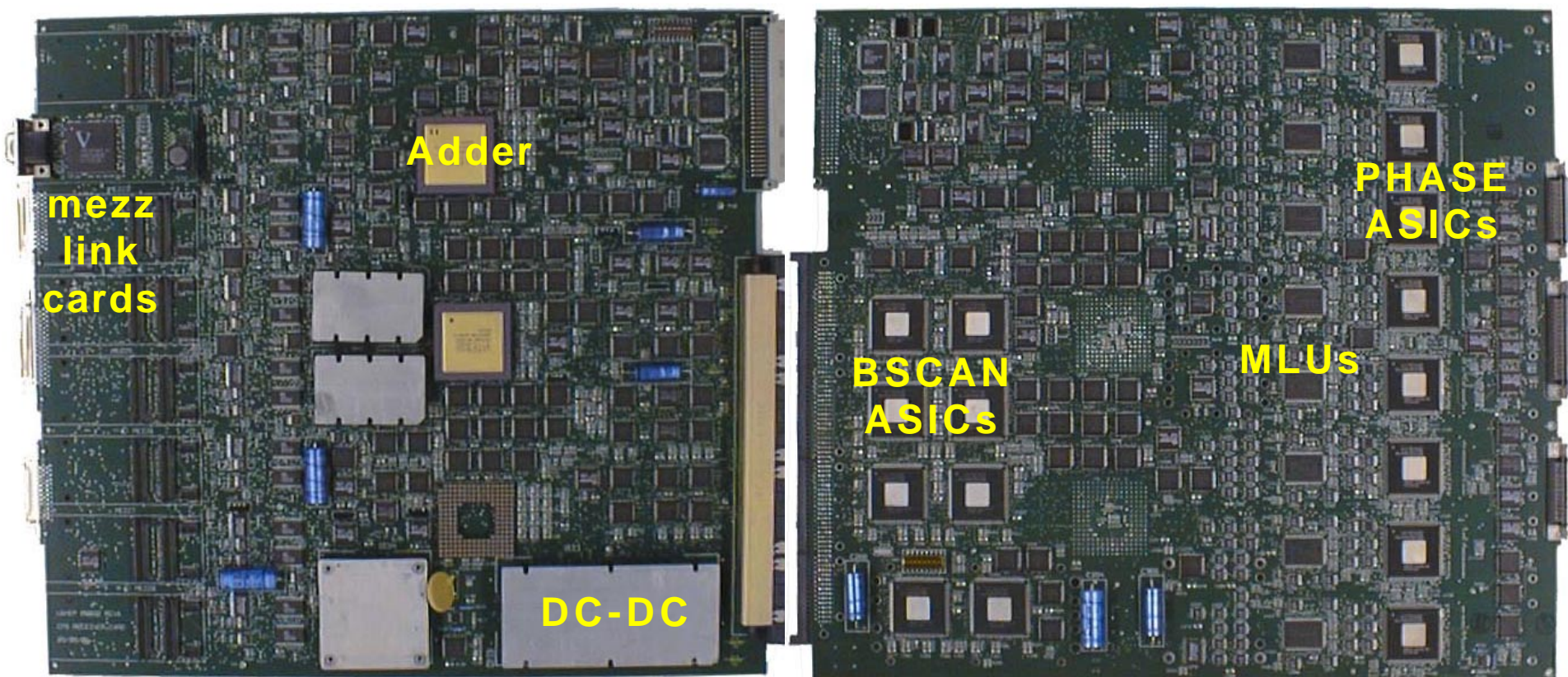
New Serial Link Test Card

Status: under test



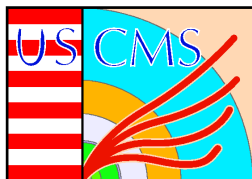
New Calorimeter Trigger Receiver Card (U. Wisconsin)

Full featured final prototype board is in test - initial results are good.
Continue to test on-board ASICs & copper link mezzanine cards

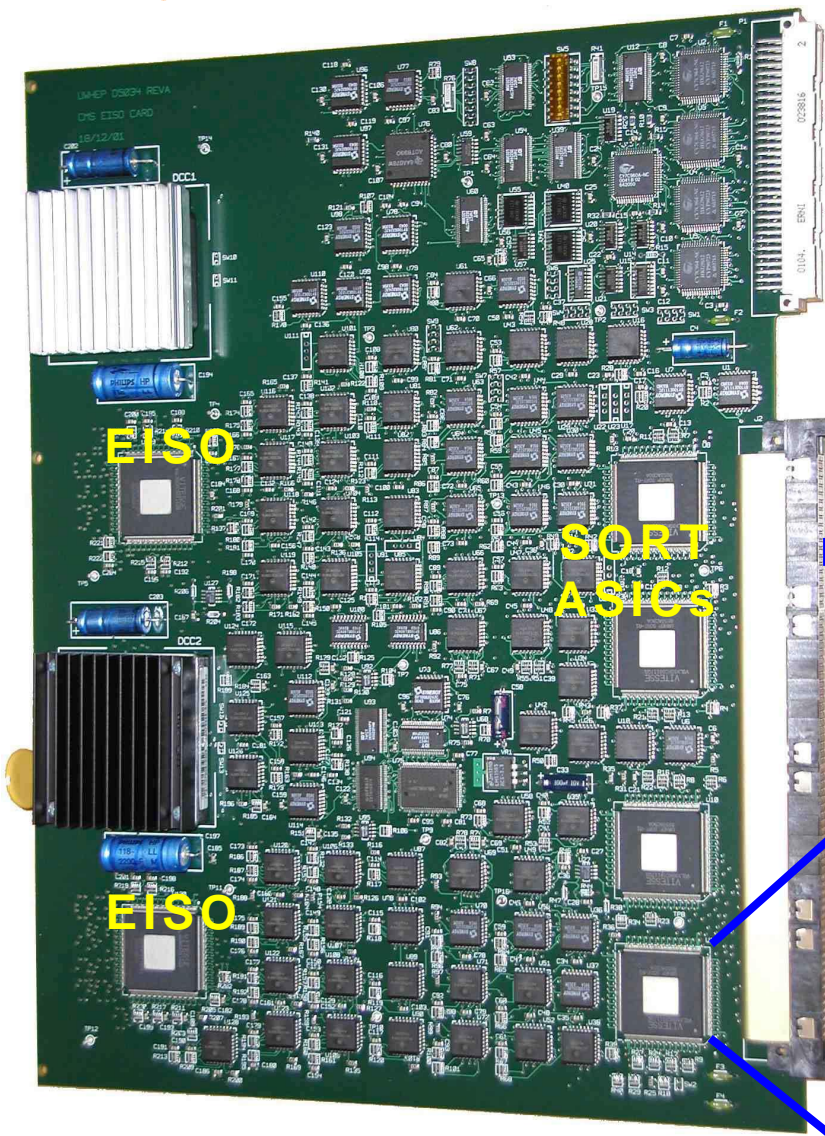


*Top side with 1 of 8 mezzanine cards
& 2 of 3 Adder ASICs*

*Bottom side with all Phase
& Boundary Scan ASICs*

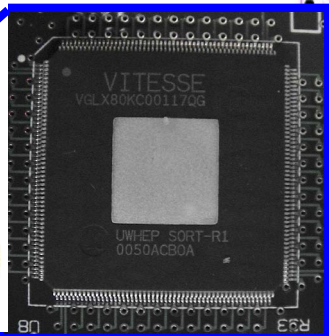
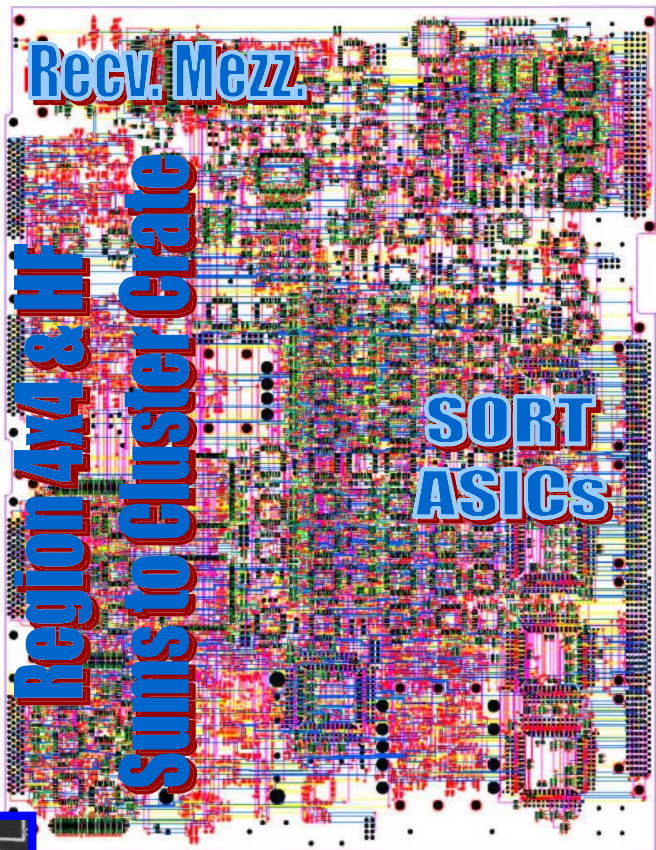


Cal. Trig. New Electron Isolation & Jet/Summary Cards (Wisconsin)



Full featured final E.I. Proto. board is finished & ready for testing.

JSC Proto. ready to build pending tests of other boards



E.I. Proto will test Electron Isolation ASICs & Sort ASICs



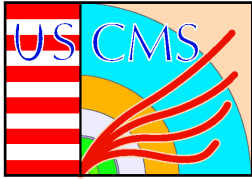
Cal Trigger Status/Plans

Second generation prototype tests underway

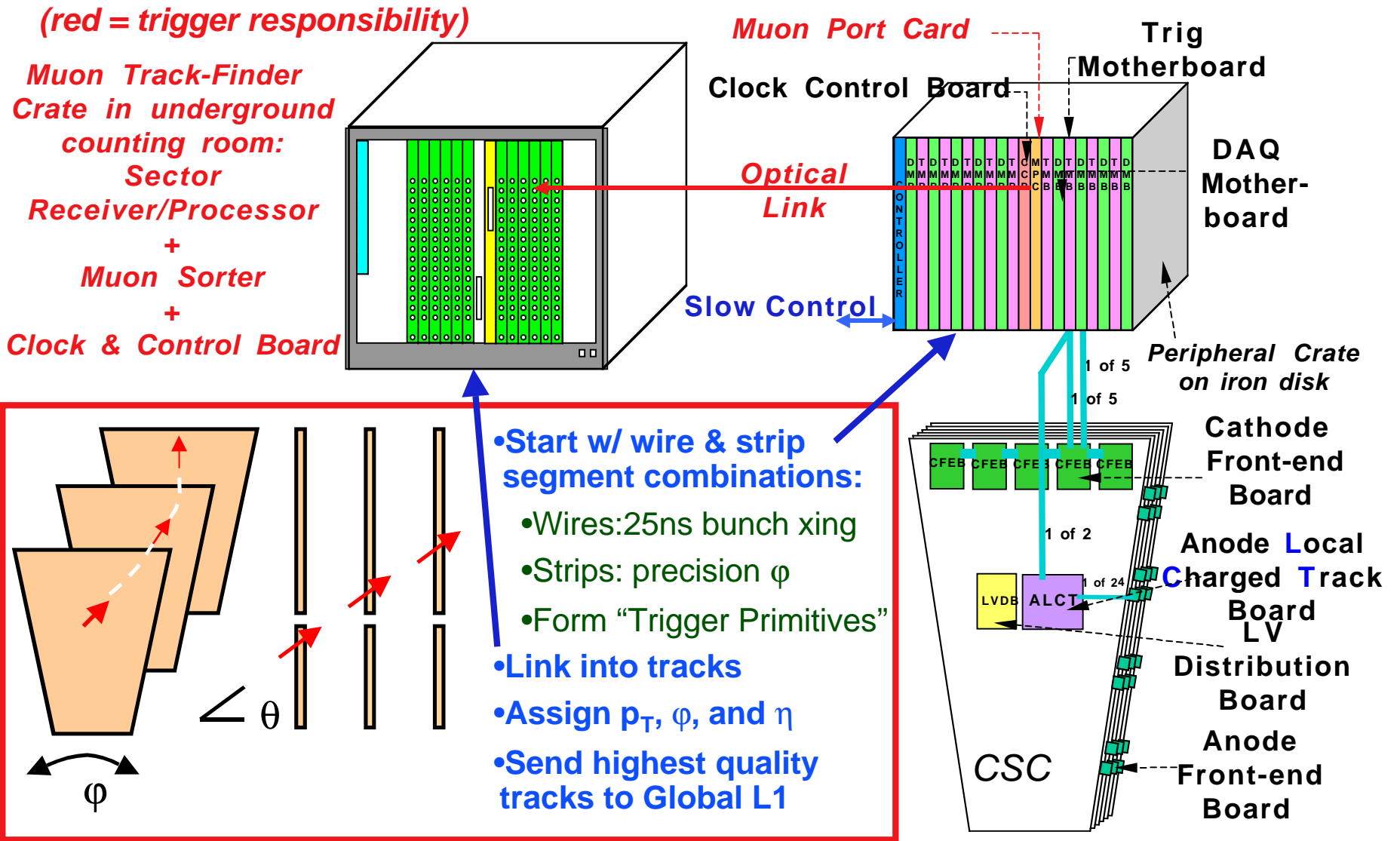
- Crate, Backplane, Clock & Control, ASICs, Receiver Card & Electron Isolation Card done & under test
- Jet/Summary Card designed & laid out
- Serial Link Mezzanine Card Receiver, Transmitter & Tester Card done & under test

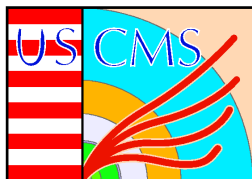
Goals for 2002

- Complete of prototype tests, validate ASICs
- Integrate Serial Links w/ECAL,HCAL front-ends
- Prototype Jet/Summary card manufacture
 - Ready for manufacture -- waiting for other board tests
- Finalize Jet Cluster crate design

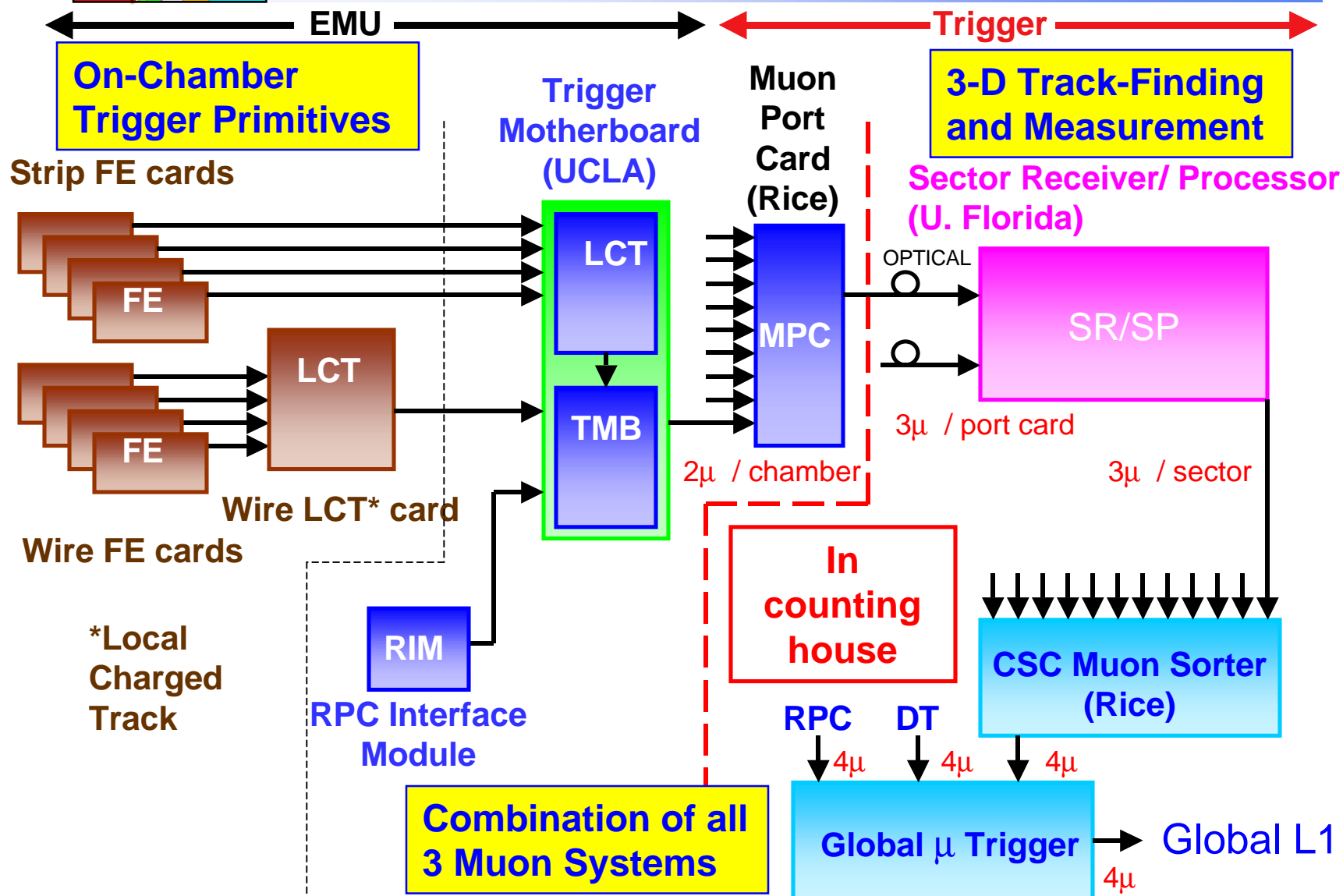


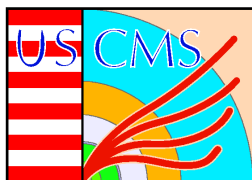
CSC Muon Trigger Overview





CSC Muon Trigger Scheme





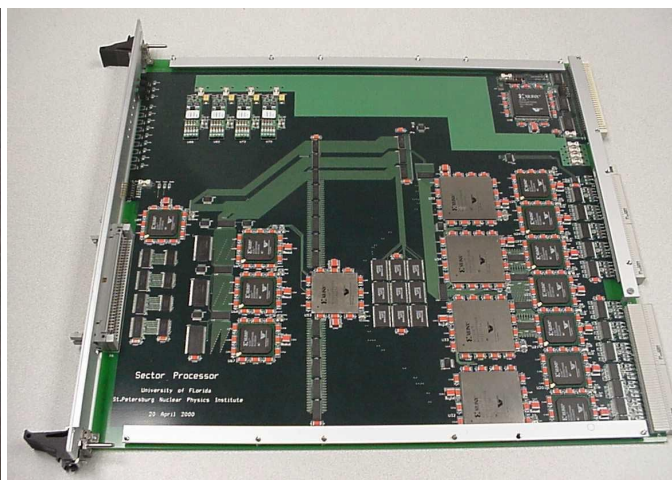
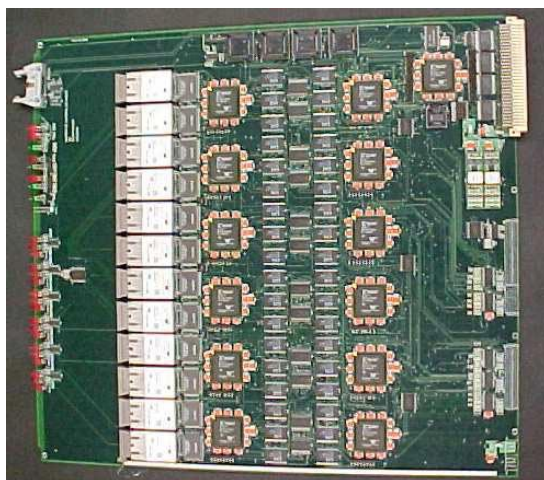
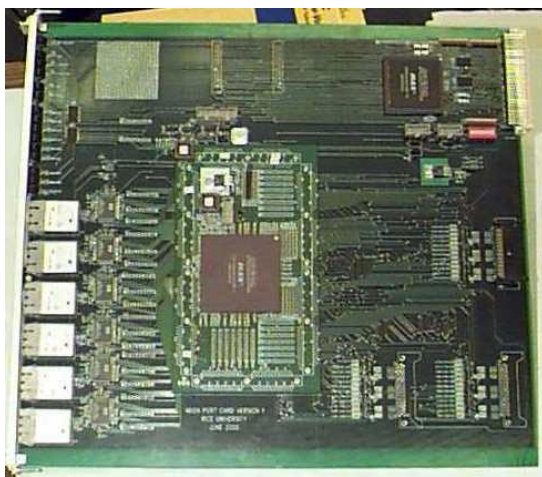
1st Muon Trigger Prototypes (Florida, Rice, UCLA)

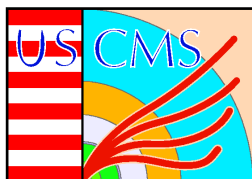
Successful CSC Trigger Integration test

- Prototype Muon Port Card, Sector Receiver, Sector Processor, Clock Board, Backplane work & communicate -- Result in 2000

ORCA full simulation working

- Agreement/use with hardware test





1st Track-Finder Crate Tests

Sector Processor
(Florida)

Sector Receiver
(UCLA)

Clock Control
Board (Rice)

Muon Port Card
(Rice)

Bit3
VME
Interface

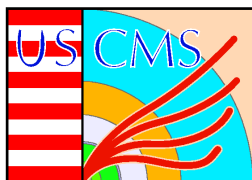
Custom
Backplane
(Florida)

Prototype
crate for
original six
crate design



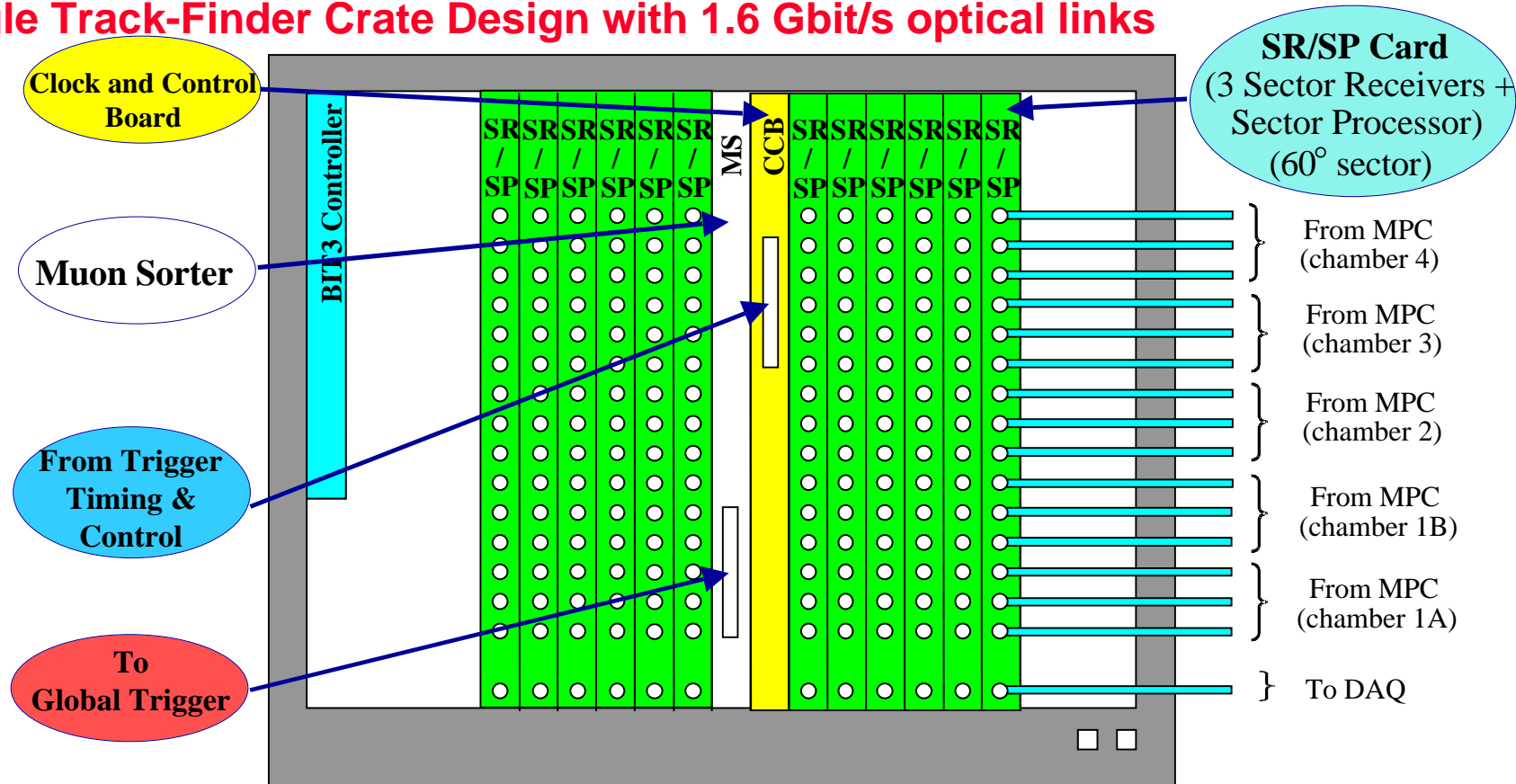
Very successful, but overall CSC front end through trigger processing latency too high -- New design in 2001

100m optical fibers

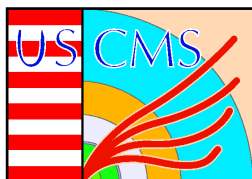


New EMU Trigger Design: U. Florida Track-Finder

Single Track-Finder Crate Design with 1.6 Gbit/s optical links

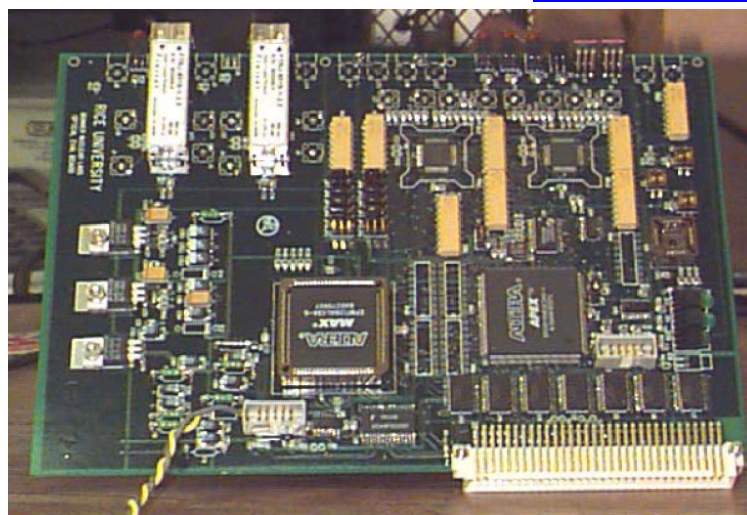
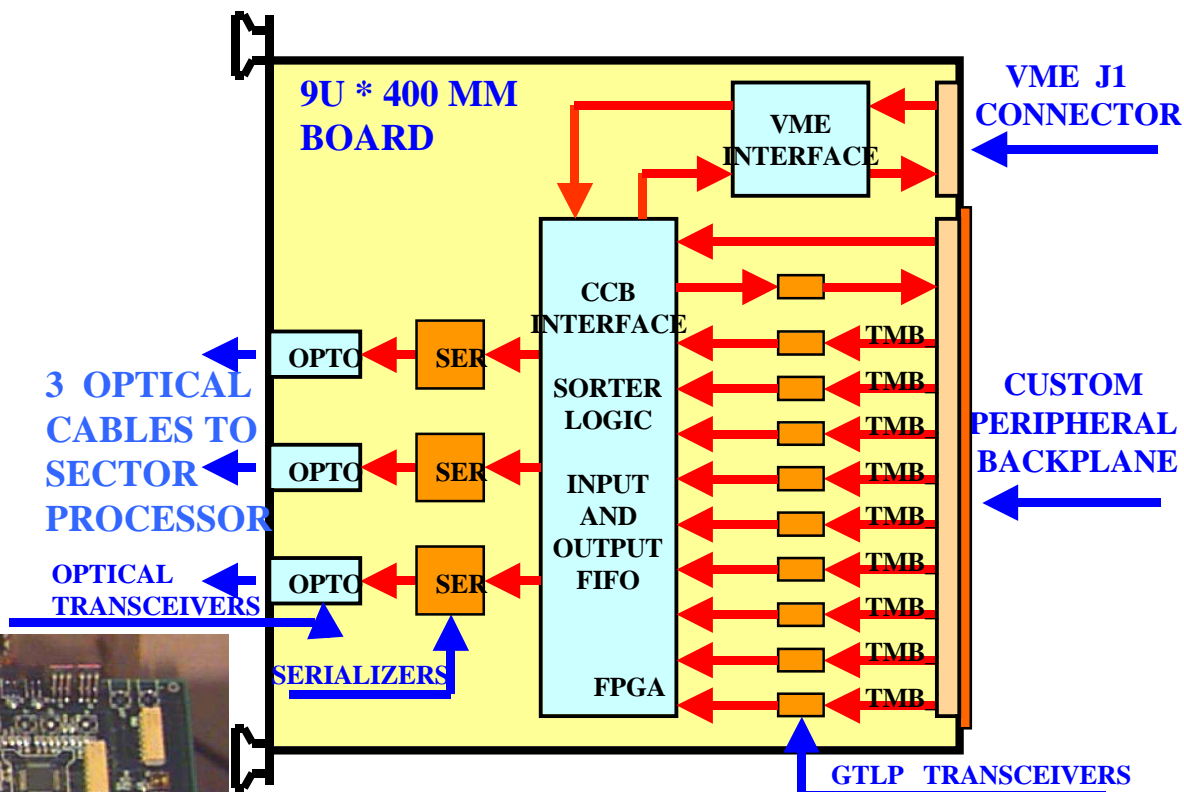


- Reduces processing time from 525 ns (old design) to 175 ns
 - Total Latency ~ 15 Bx (from input of SR/SP card to output of MS card)
- Crate Power Consumption ~ 1000 W • 16 Optical connections per SR/SP card
- Custom Backplane for SR/SP ↔ CCB and MS connection



New Muon Port Card Design & Optical Link Tests (Rice)

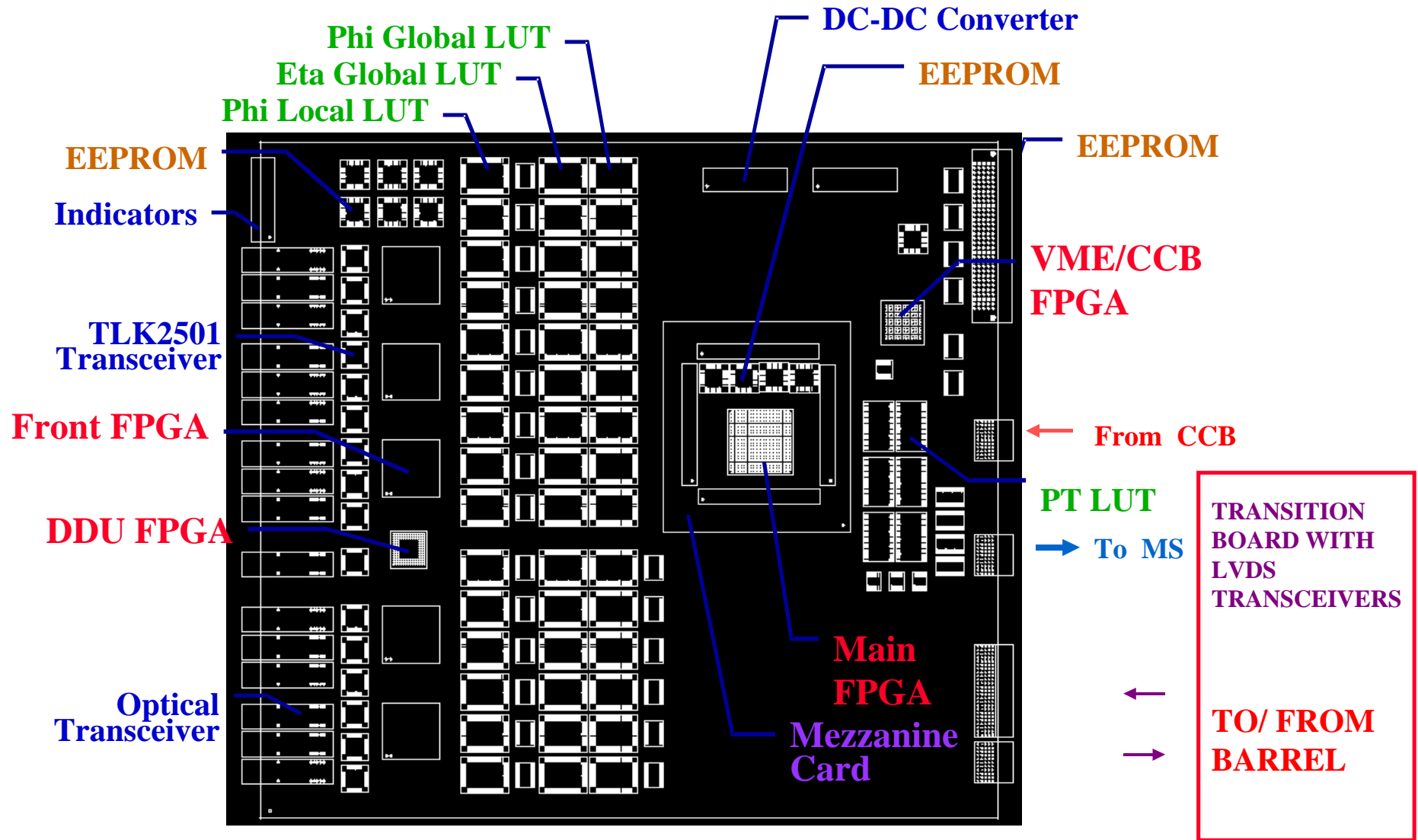
New MPC Design uses new high speed links (TLK2501) to send one muon per optical fiber (needed for new compact track-finder design)



Optical Link Radiation Tests:
Three serializers: up to 270 kRad TID. No permanent damage or SEU
Two Finisar optical modules: No errors up to 70 kRad. Failed at 70kRad (well above ~10 kRad TID inner CSC dose for 10 years)

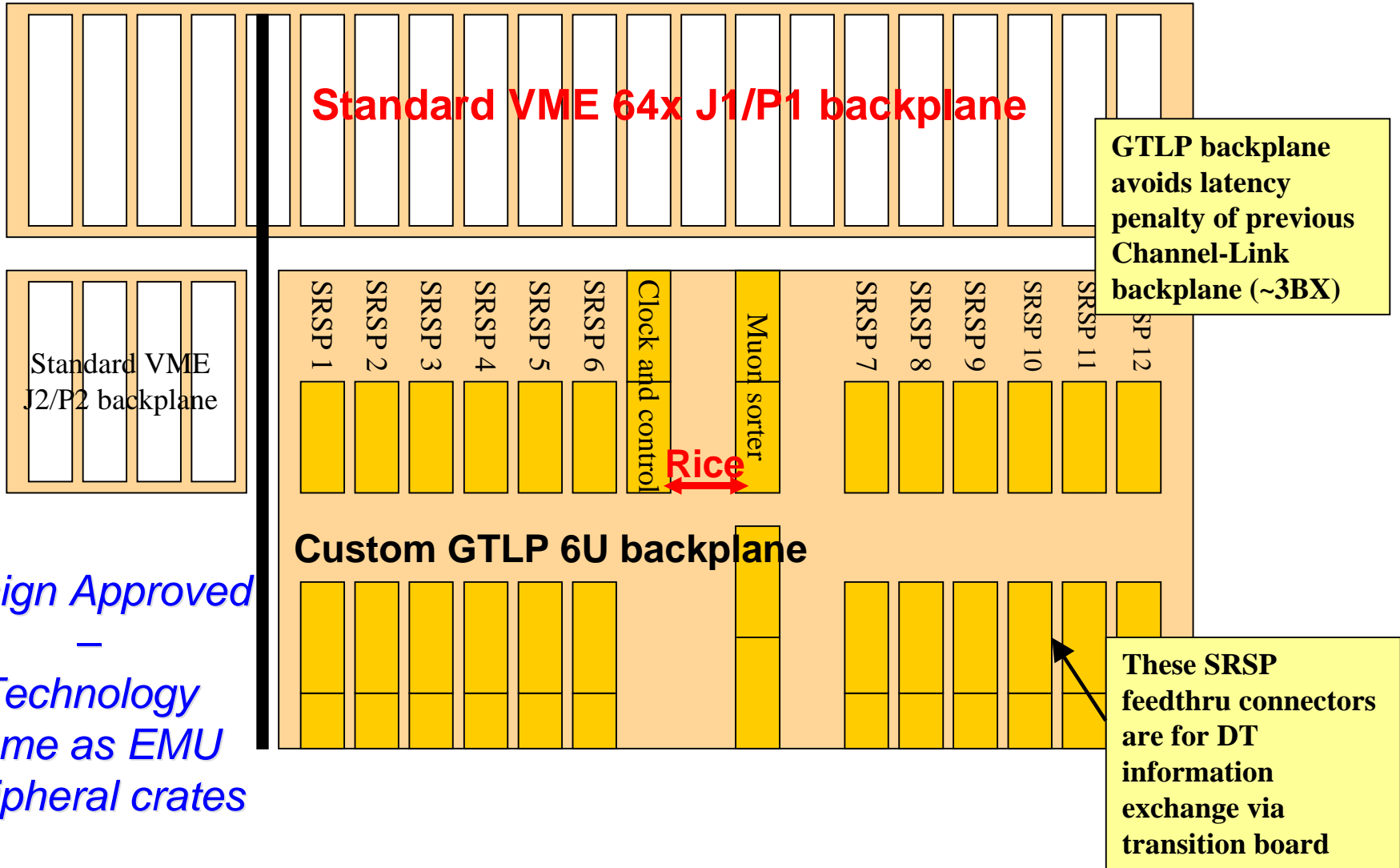


SR/SP 2002 Board Layout (U. Florida)





CSC Track Finder Backplane (U. Florida)

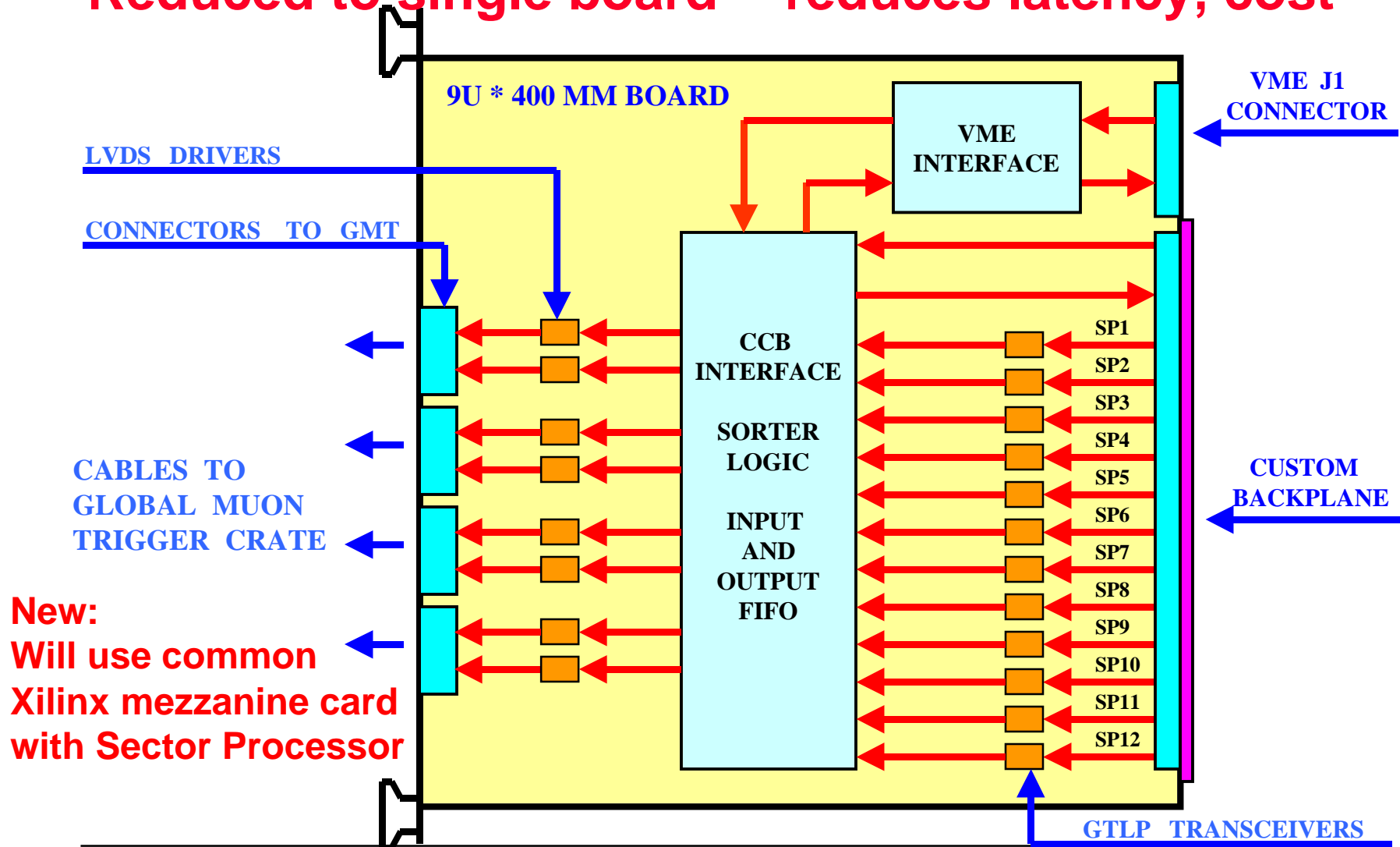


Design Approved
—
Technology same as EMU peripheral crates



New Muon Sorter Design (Rice)

Reduced to single board -- reduces latency, cost





CSC Trigger Status/Plans

Prototype 1 tests now complete

Prototype 2 and production follow EMU components to optimize technology

MPC, SP, CCC modules, backplane* milestones:

- **Apr-02 Prototype 2 designs done ✓**
 - Freeze CSC-DT interface
 - Determine DAQ interface w/ EMU readout
- **Nov-02 Prototype 2 construction done**
- **Apr-03 Prototype 2 testing done (begin EMU integration)**
- **Sep-03 Final designs done**
- **Oct-04 Production done**
- **Apr-05 Installation done**

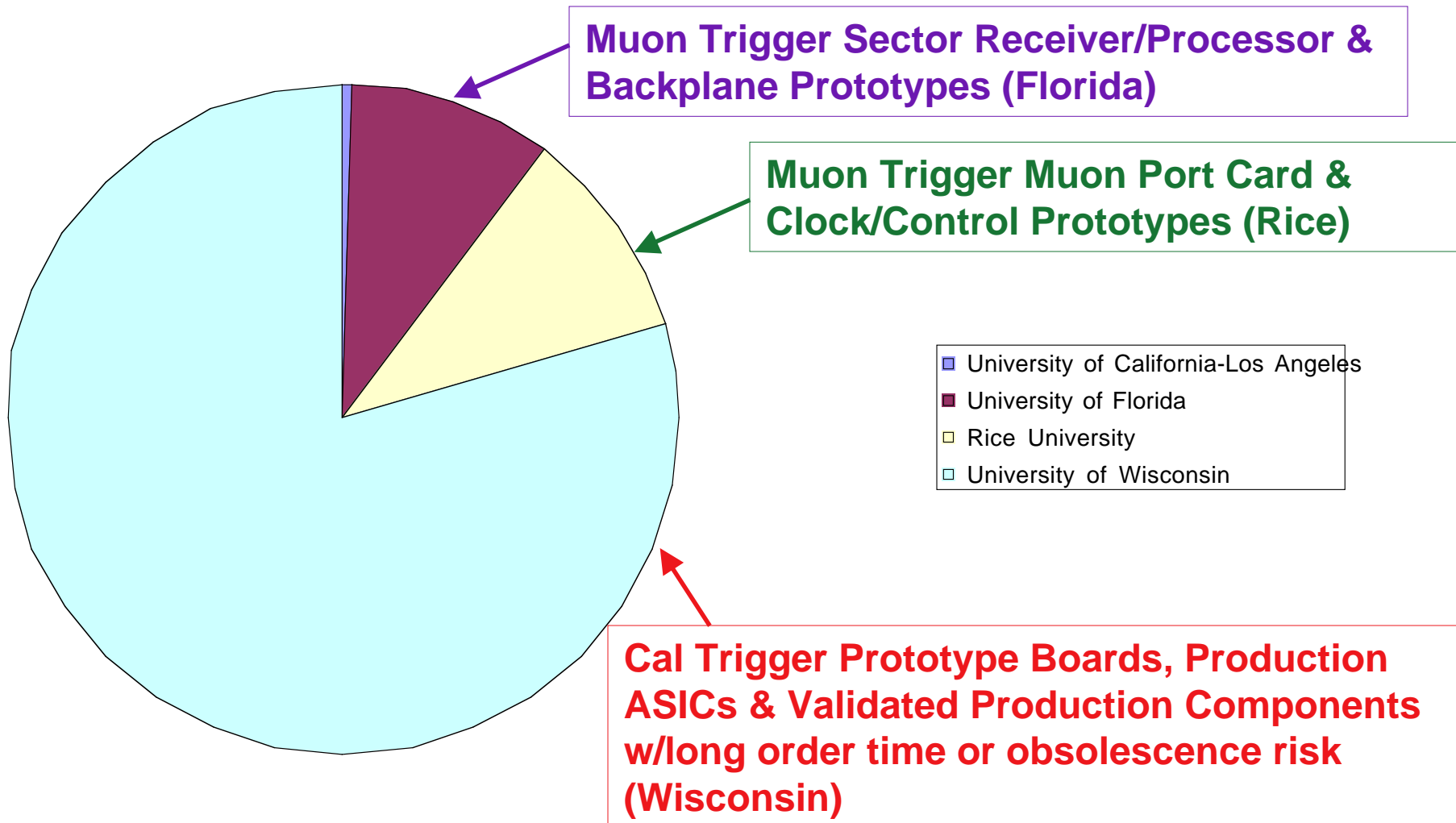
(*backplane schedule ~3 months ahead of above dates to provide platform for testing and integration)

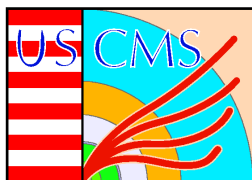
Muon Sorter module: only 1, design by Jan-04



US Trigger FY02 Planning

Trigger SOWs FY02 -- \$1.7M





Recent Trigger Milestone Performance (v31)

RCT Delays of 3-5 months:

- Reorganized board schedule to accelerate Vitesse ASIC testing

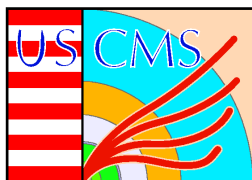
- Delay JSC since not needed for ASIC tests

- Success with 1st generation prototypes → make 2nd generation prototypes preproduction

- Longer design time delays testing

- Saves time later in schedule

Milestone	v31 Base	Current Start	Variance	'99	'00	'01	'02	'03
☐ Trigger Subsystem (WBS 1.3.1)	NA	Nov 30 '99	0 days					
Design of Final Sort ASIC	Nov 30 '99	Nov 30 '99	0 days	●				
Review of Calorimeter Trigger Control and Reac	Nov 30 '99	Nov 30 '99	0 days	●				
TK: SP Proto Design (Florida)	Nov 30 '99	Nov 30 '99	0 days	●				
CSC: MPC Proto Delivery (Rice)	Jul 31 '00	Jul 31 '00	0 days		●			
Review of Integration of Calorimeter Trigger Proc	Nov 30 '00	Nov 30 '00	0 days			●		
Submit Trigger Technical Design Report (TDR)	Dec 31 '00	Dec 31 '00	0 days			●		
RCT: CCC Proto Test Complete	Dec 31 '01	Jul 31 '02	148 days				●	●
Finish Trigger Final Prototype Design	Dec 31 '01	Dec 31 '01	0 days				●	
GCT: System Design Complete Not US	Dec 31 '01	Aug 31 '02	171 days				●	●
CSC: Bckpl Specified (DT Info)	Dec 31 '01	Dec 31 '01	0 days				●	
Regional Cal. Trig. - RC Proto Test Complete	Feb 28 '02	Jul 31 '02	109 days				●	●
RCT: ASIC Proto Test Complete	Mar 31 '02	Jul 31 '02	87 days				●	●
RCT: Bckpl Proto Test Complete	Mar 31 '02	Jul 31 '02	87 days				●	●
RCT: JSC Proto Test Complete	Apr 30 '02	Sep 30 '02	109 days				●	●
RCT: Electron ID Proto Test Complete	Jun 30 '02	Jun 30 '02	0 days				●	
Finish Trigger Final Prototypes	Jun 30 '02	Jun 30 '02	0 days				●	
CSC: C&CB Proto Test Complete	Sep 30 '02	Sep 30 '02	0 days				●	
RCT: CCC Prod Test Complete	Oct 31 '02	Oct 31 '02	0 days				●	
Finish Trigger Final Prototype Test Complete	Dec 31 '02	Dec 31 '02	0 days				●	
GCT: Integration Test Complete	Dec 31 '02	Dec 31 '02	0 days				●	
CSC: SR/SP Proto Test Complete	Mar 31 '03	Mar 31 '03	0 days				●	
CSC: MPC Proto Test Complete	Mar 31 '03	Mar 31 '03	0 days				●	
RCT: RC Prod Test Complete	May 31 '03	May 31 '03	0 days				●	
Finish Trigger Pre-Prod Design & Test	Jun 30 '03	Jun 30 '03	0 days				●	



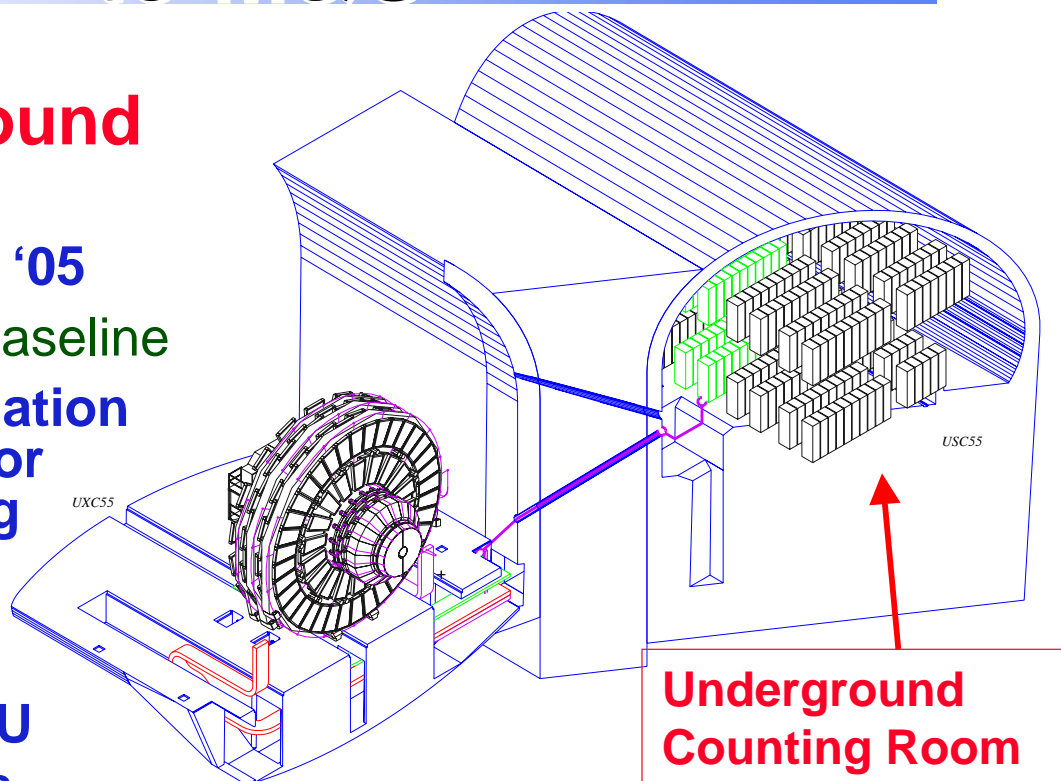
Completion & Transition to M&O

Installation in Underground Counting Room

- Expect access by March '05
 - Delay of 1 year from baseline
- Sufficient time for installation & some testing but not for complete commissioning with detectors

Slice Test (on surface)

- With both HCAL and EMU
- Verify trigger functions & interfaces by testing w/detectors on surface at CERN.
- Suggest as substitute for commissioning completion step.
- Will check as much on surface before gaining access to underground facilities.
- Planned for October '04 - March '05





Baseline Trigger L2 Task Schedule & Updates

Tasks	start	finish	new
• Produce TDR	8/00	12/00	✓
• Design Final Prototypes	11/00	12/01	✓
• Construct Final Prototypes	6/01	6/02 ⇒ 11/02	
• Test/Integrate Final Prototypes	12/01	12/02 ⇒ 4/03	
• Pre-Production Design & Test	6/02	6/03 ⇒ 11/03	
• Production	12/02	6/04	
• Production Test	6/03	11/04	
• Trigger System Tests	5/04	5/05	
• "Slice Test" (NEW) ←	10/04	3/05	←
• Trigger Installation	3/05	9/05	←
• Integration & Test w/DAQ & FE	6/05	12/05	←
• Maintenance & Operations	10/04	-----	←

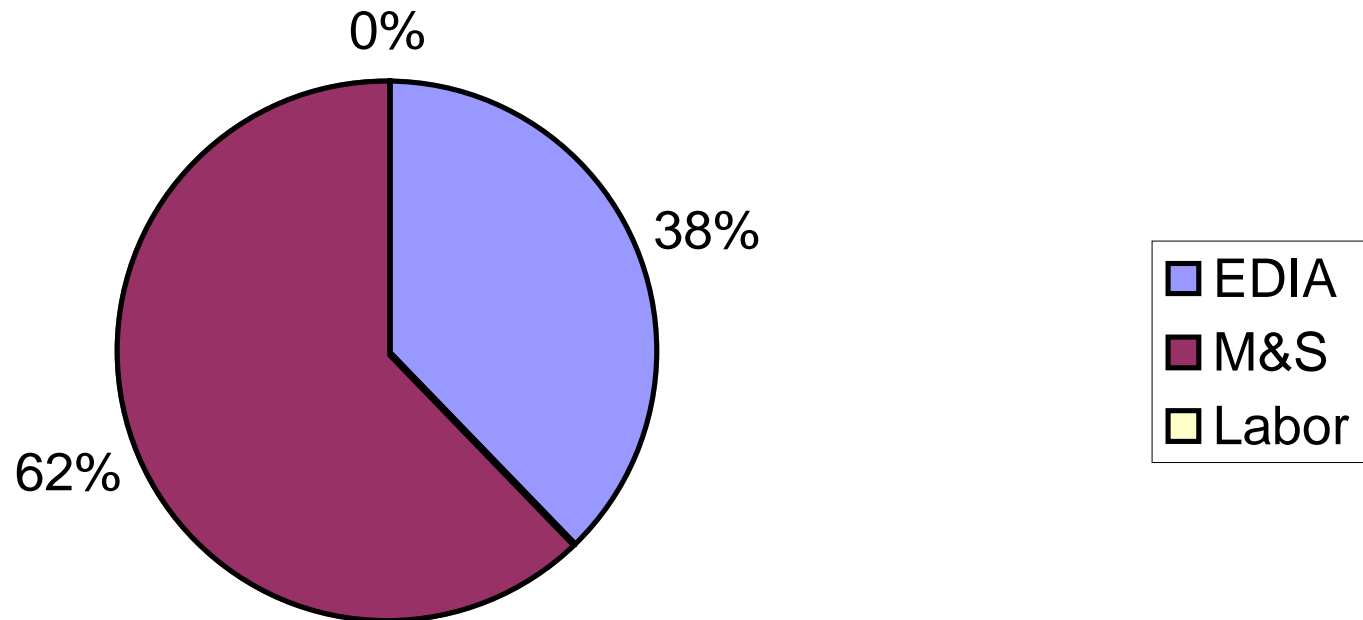
6 months civil engineering delay of installation date

- With respect to date reported at Lehman '01

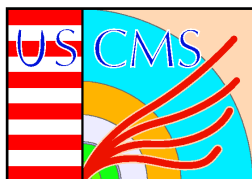


US Trigger Estimate-to-Complete

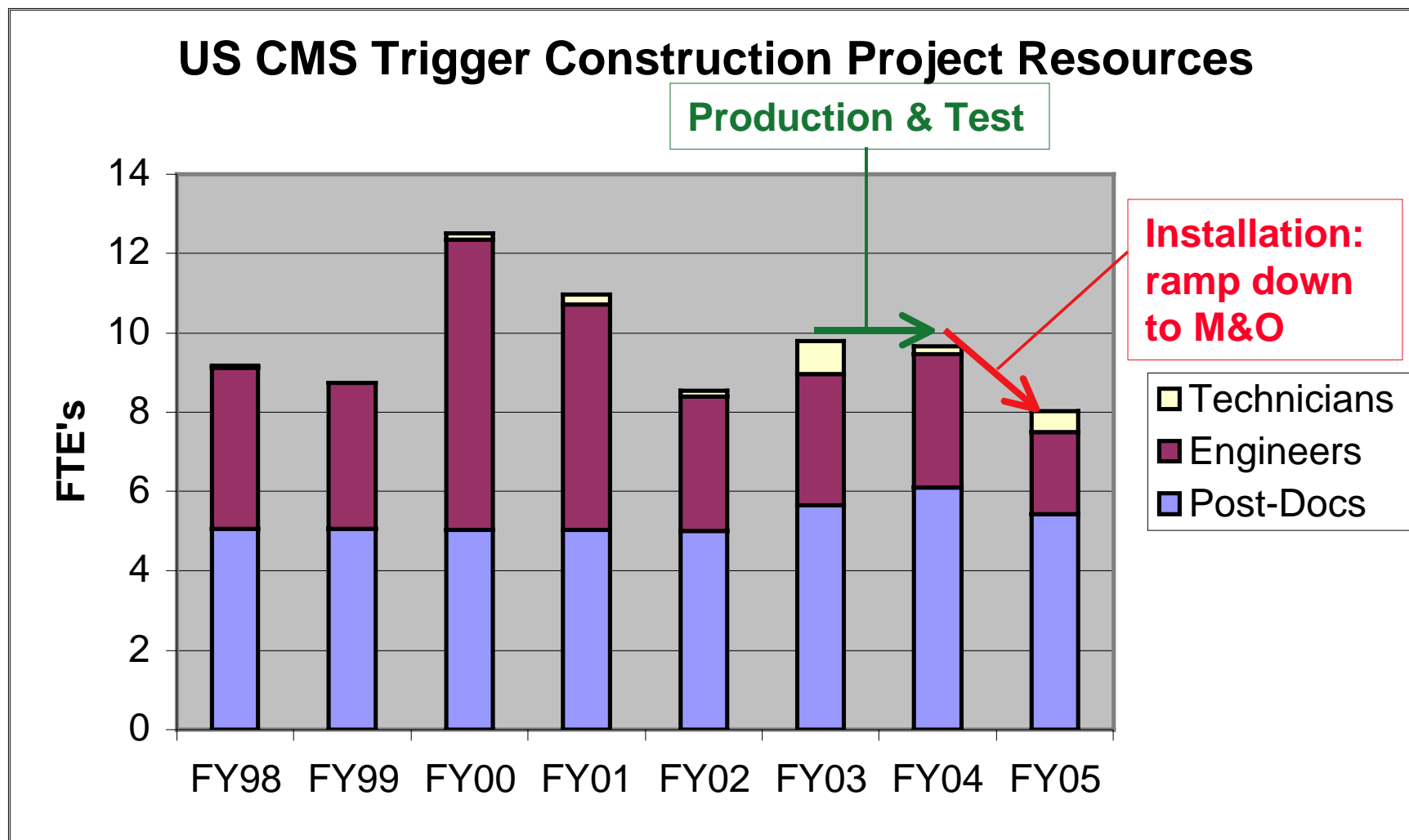
US Trigger Estimate-to-Complete = \$4.6M AY
1998 Project Baseline Total Cost = \$7.6M AY
2002 Project Total Cost = \$8.5M AY



As of May '02 Trigger Project is 46% Complete
Costs up 12% over '98 baseline (50% contingency)

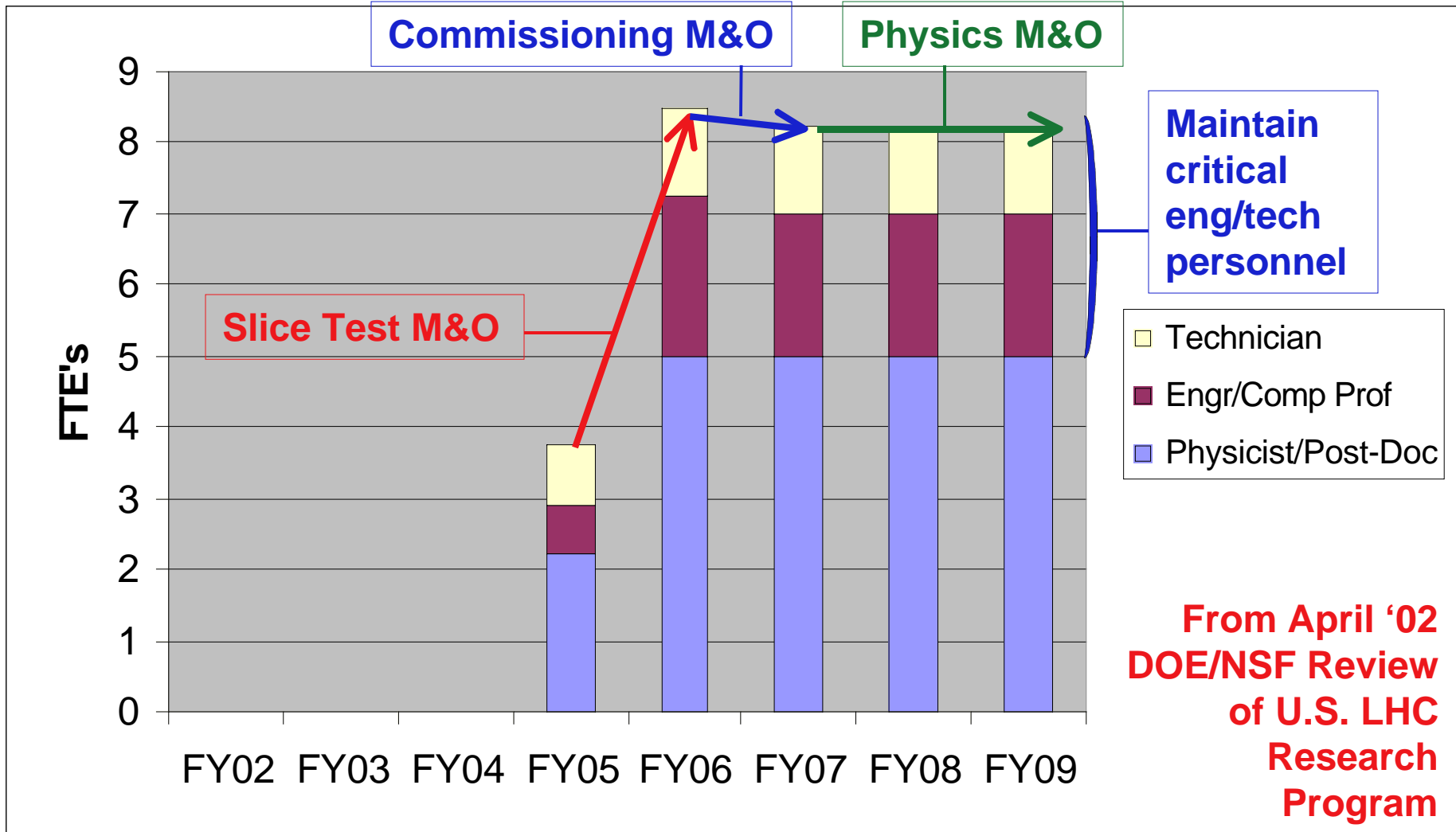


US TRIG Project Resources (FTE's)



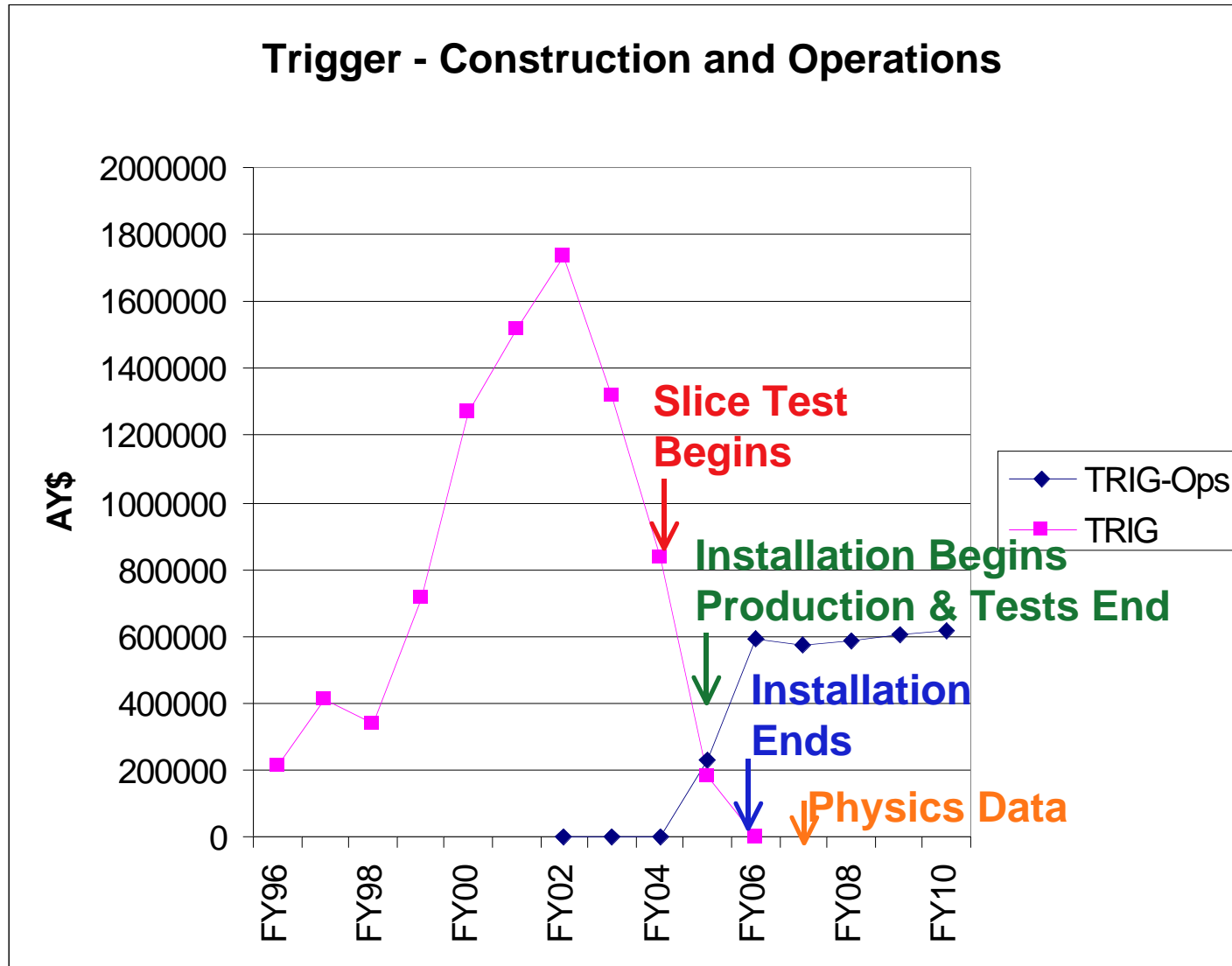


US Trigger M&O Resources





Trigger Commitments





Concerns

Installation Schedule

- New schedule has reduced installation time
- Significant time needed for integration in a synchronous pipelined system.

Base Program Manpower

- Major effort on trigger software required
 - Tasks include board testing, monitoring/controls, diagnostics, configuration downloading and documentation, modeling, physics simulation, etc.
- Major effort on testing & installation
 - Planned as activity of base program manpower
- New Major Effort on “Slice Test”
 - Motivated by installation delay
 - Also needs base program manpower



Conclusions - Trigger

Calorimeter Trigger

- All second generation prototype boards and ASICs built and under test
 - Except jet summary card -- ready for manufacture
- Initial test results look good
- Integration tests w/ECAL,HCAL start this Fall

Muon Trigger

- All second generation prototype boards and their FPGA logic are designed
 - Construction is starting
- Integration tests start w/EMU next Spring