WBS 3.1 - Trigger

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CMS Trigger Project Manager

DOE/NSF Status Review

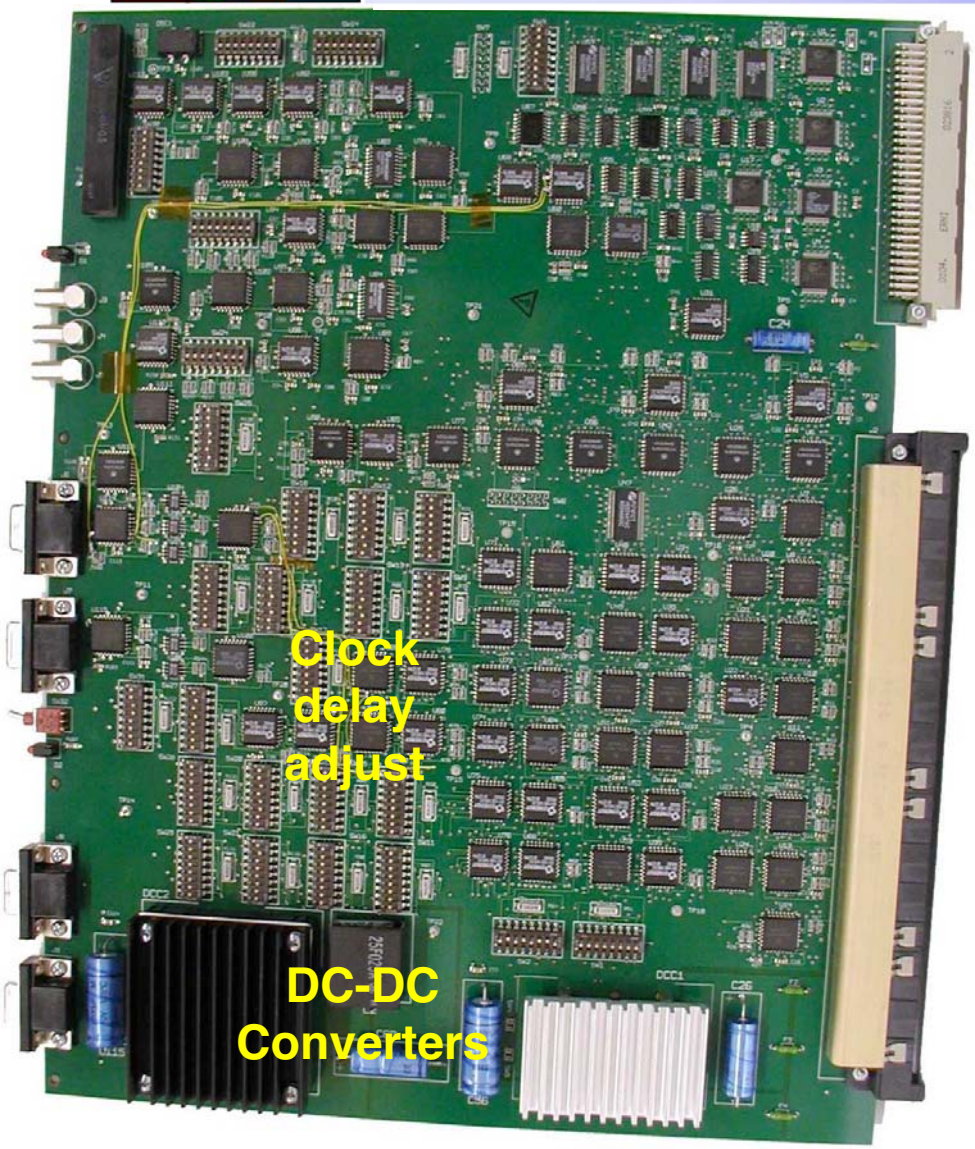
November 20, 2003

This talk is available on:

http://hep.wisc.edu/wsmith/cms/Trig_Lehman_Nov03.pdf

Pre-Production Clock & Control Card

Wisconsin



- Fans out 160 MHz clock & adjusts phase to all boards
- Design validated - with small changes, layout and routing of production version completed.
- *Manufacture Begun - All PCBs delivered by November 26*

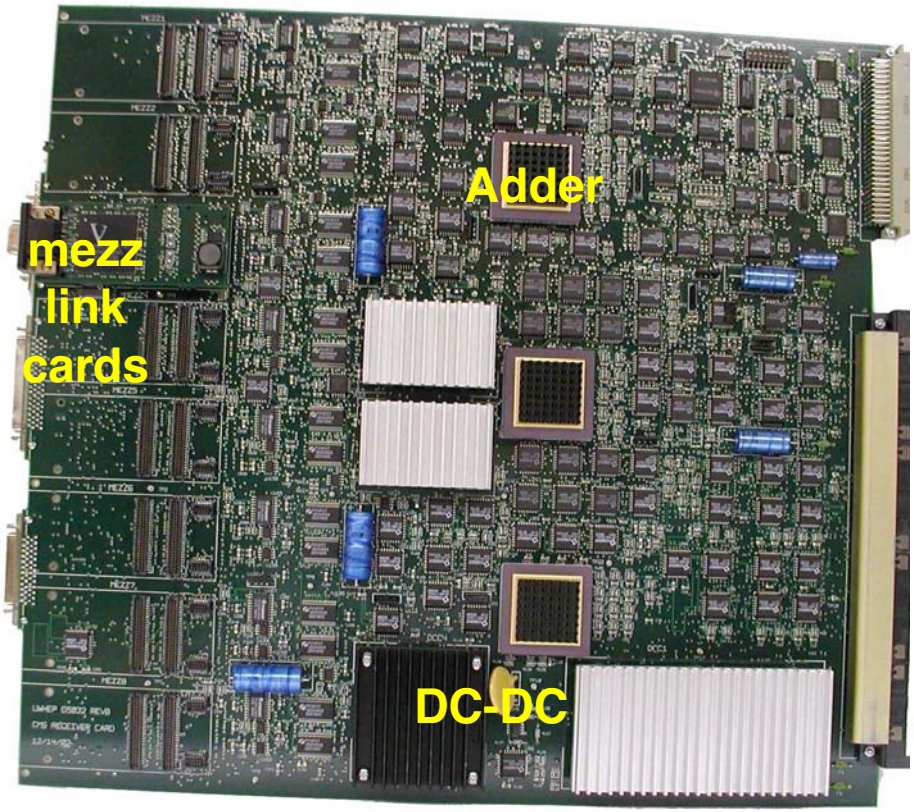
Receiver Cards

Wisconsin

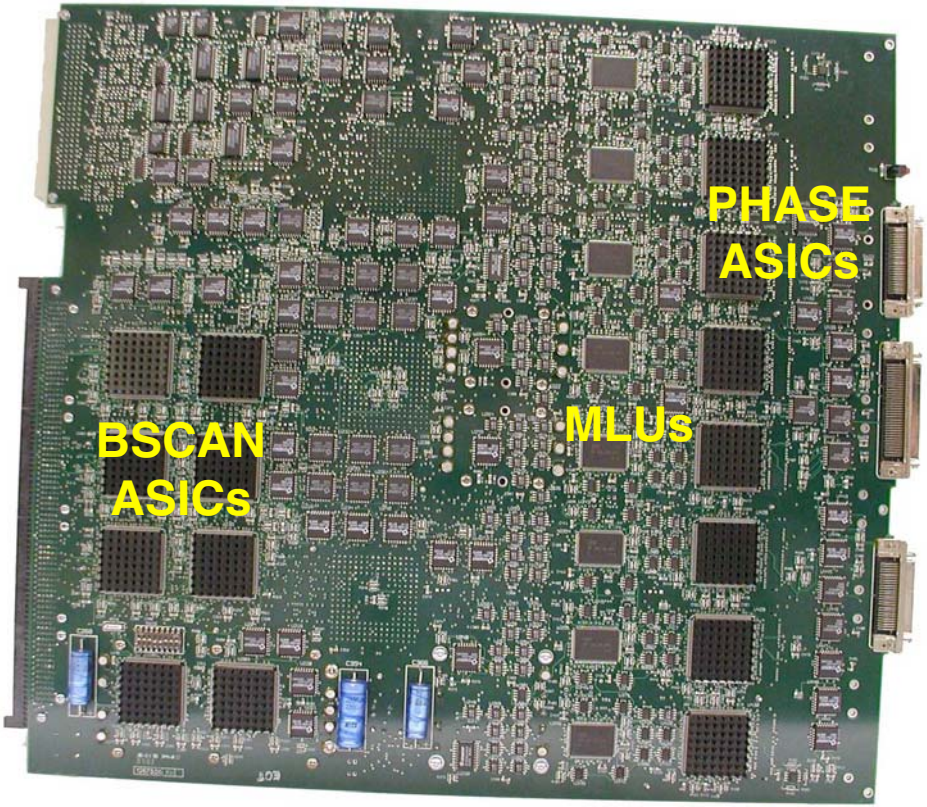
Pre-Production full feature RC and all ASICS fully validated.

Full quantity of mezzanine link cards produced and under test at UW.

RC production started, PCBs Nov. 21, 6 assembled for eval.: Dec.13



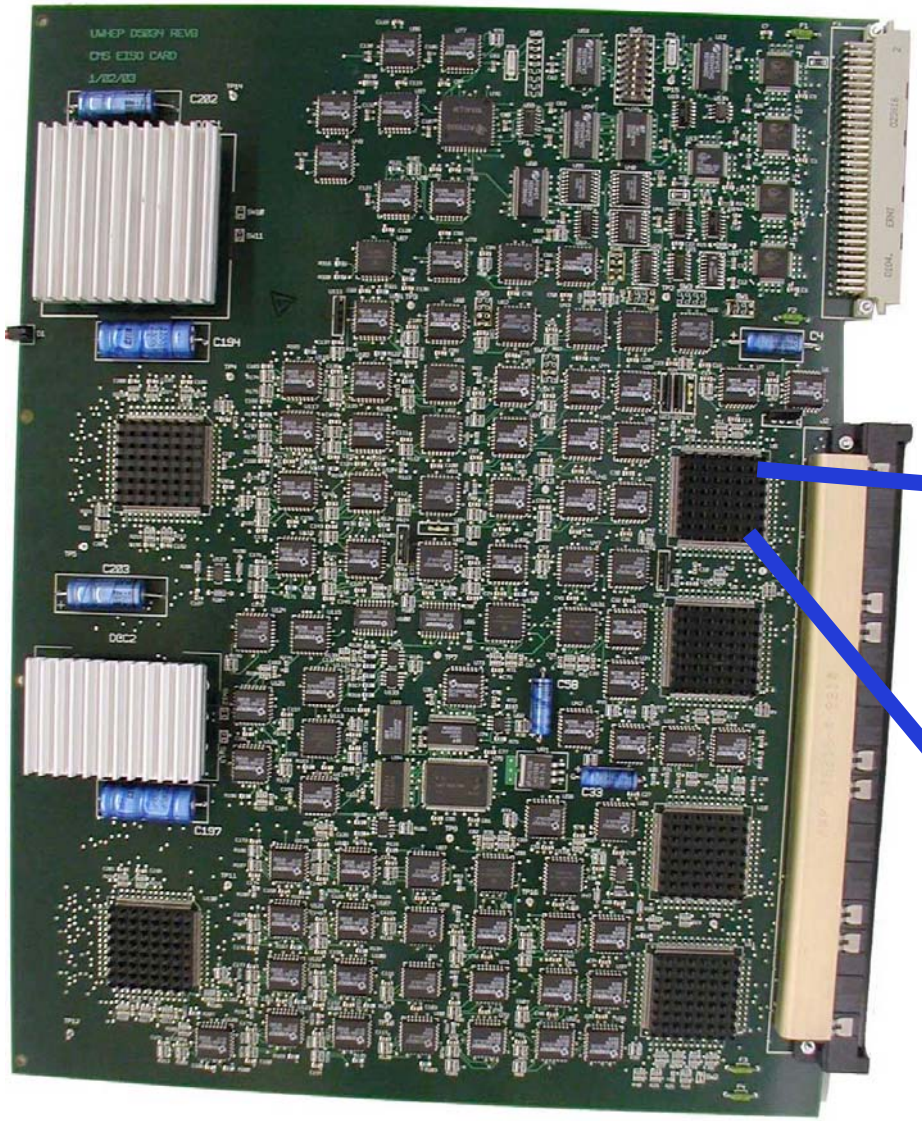
Top side with 1 of 8 mezzanine cards & 2 of 3 Adder ASICs



Bottom side with all Phase & Boundary Scan ASICs

Pre-Production Electron Isolation Card

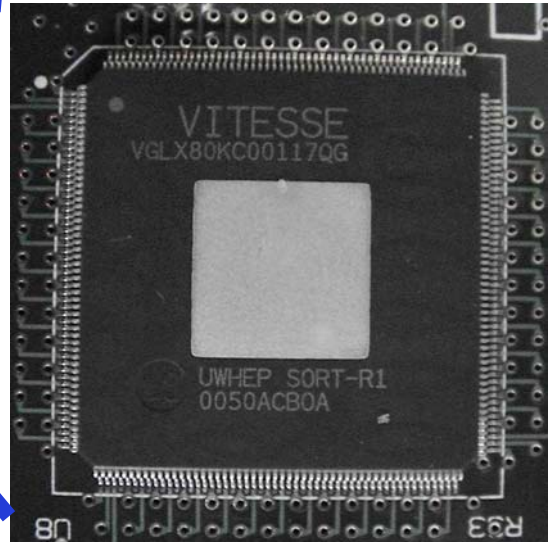
Wisc.



Full featured final prototype board is fully validated and production underway, first bare boards expected. 6 evaluation boards expected 5 Jan 04

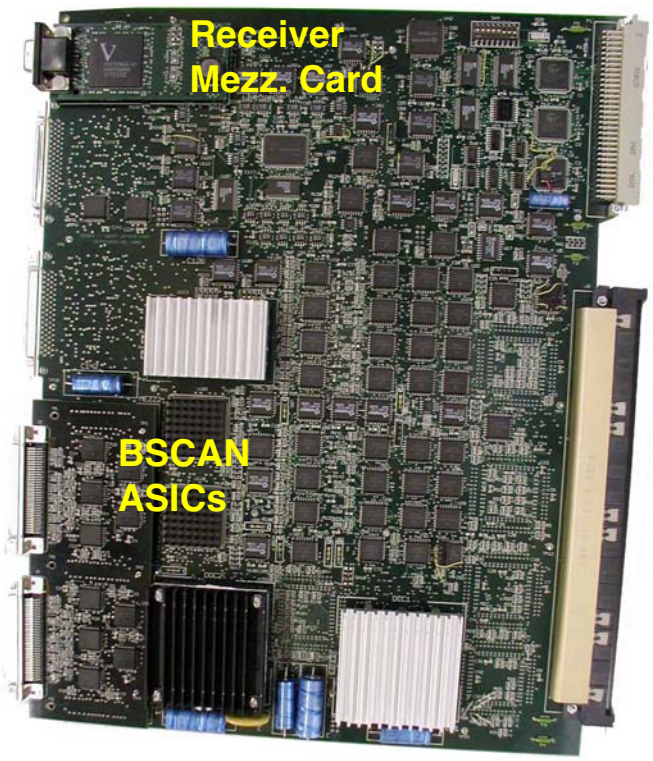
Electron ID & Sort ASICs validated and production complete

All PCBs expected by Nov. 26

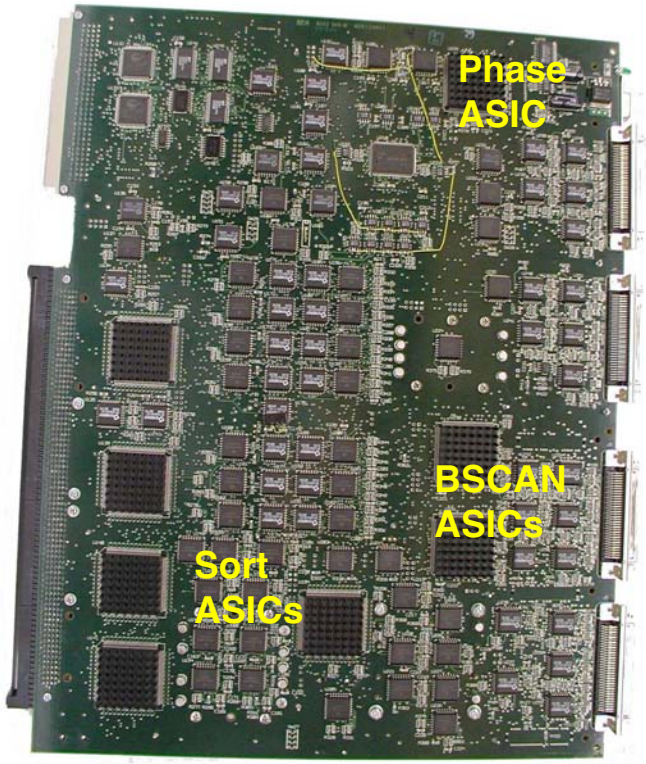


Jet/Summary Card

Wisconsin



Backplane:
Two e/γ
per region.
Region E_T
Sums



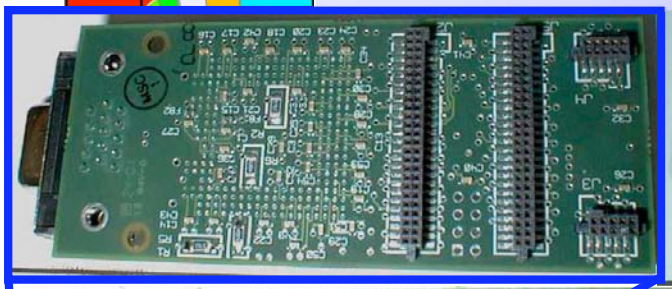
Cables
To GCT
(2 on
Mezz.
Card -
Proto
Assem.)

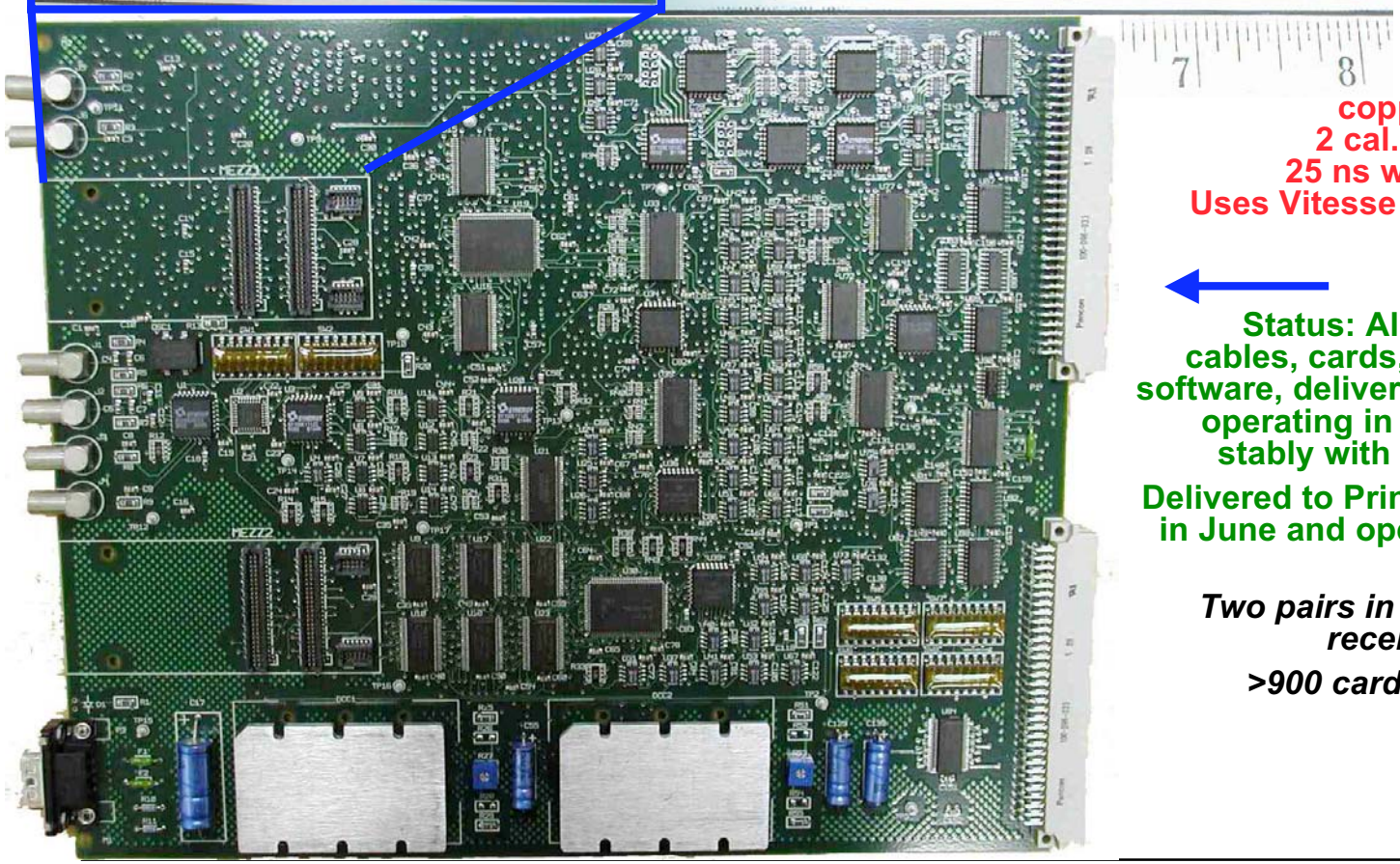
Full function prototype manufactured and under final tests

- Uses SORT ASICs to find top four e/γ, threshold for muon bits, both to GCT
- Region energies to GCT
- Absorbs HF functionality with Rec. Mezz. Card, HF sent to GCT
- Full crate test - all output paths verified, electron sort, jet output all OK
- Integration test with GCT Done - Change in termination - Production to start shortly

Cal. Trig. 4 Gbaud Copper Link Cards & Serial Test Card

Wisc.





Compact Mezzanine Cards for each Receiver Card accept 4 x 20 m 1.2-Gbaud copper pairs transmitting 2 cal. tower energies every 25 ns with low cost & power. Uses Vitesse Link Chips (7216-01).

Serial Link Test Card

Status: Already commissioned, cables, cards, 48V PS, and support software, delivered to CERN in March, operating in ECAL Electronics lab stably with no errors for months.

Delivered to Princeton for HCAL tests in June and operating stably with no errors since.

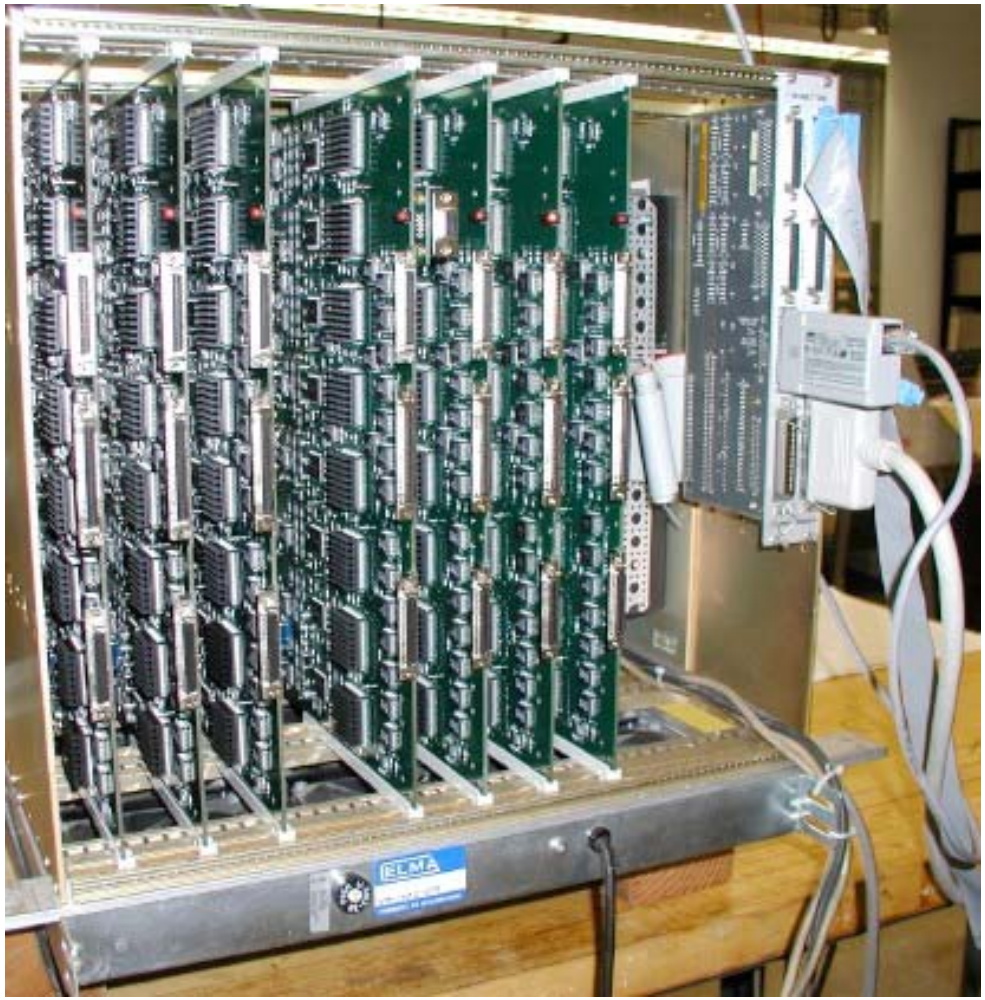
Two pairs in use @ UW for testing receiver mezzanine cards,

>900 cards of 1422 fully tested.

First Full RCT Crate

Wisconsin

18 Such Crates make up the full RCT System covering $|\eta|<5$ & $0 < \phi < 2\pi$.



Rear: Receiver Cards

Front: Electron, Jet, Clock Cards

Calorimeter Trigger Status/Plans

Pre-Production full function prototype tests

- CCC, EISO, RC, all ASICs Validated
- JSC nearly validated

Production Underway

- All Receiver Mezzanine Cards in hand (1422) and >900 tested successfully
- All ASICs made
- Production Begun for RC, EIC, CCC, Backplane, Crate

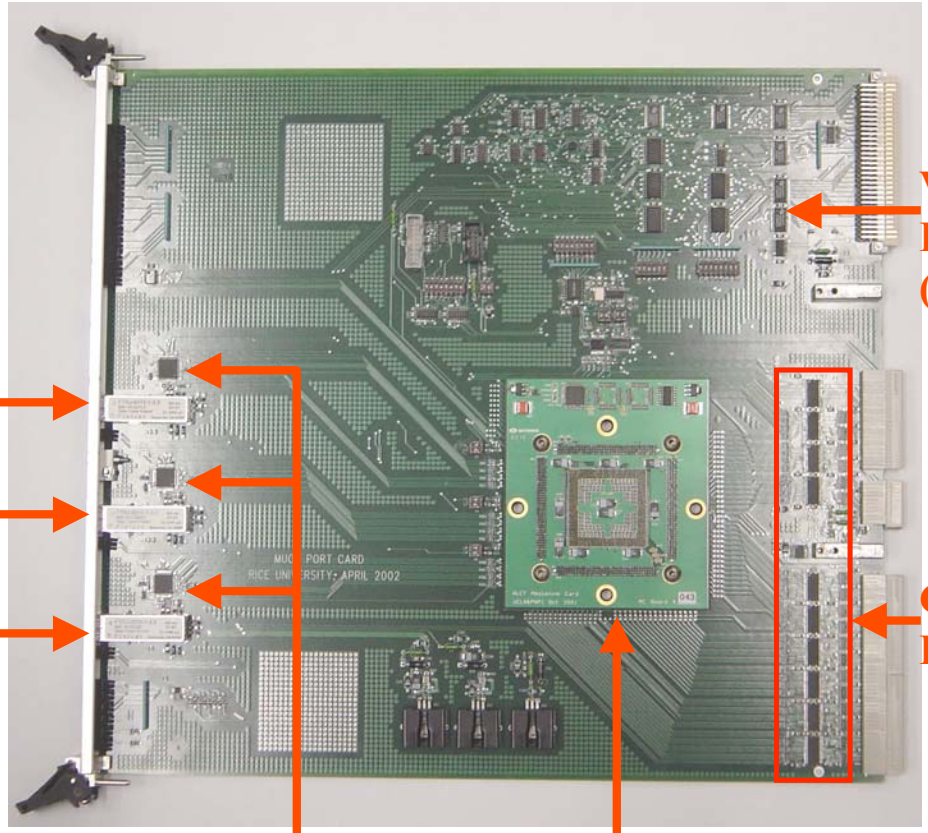
Activities

- Full production tests underway
  - Software in use and more being readied
  - Testing plan being refined
  - Boards being made
- Integration and surface test beginning 2004
  - STC's at CERN and Princeton
  - Integrated JSC output with GCT last August
  - Ship full crate to CERN for participation in HCAL surface test (2004)

Calorimeter trigger project is on track.

Muon Port Card

Rice



6 boards were fabricated and assembled in summer 2002

Tested MPC standalone (sorter logic) and with one and two Trigger Motherboards and full-size custom backplane

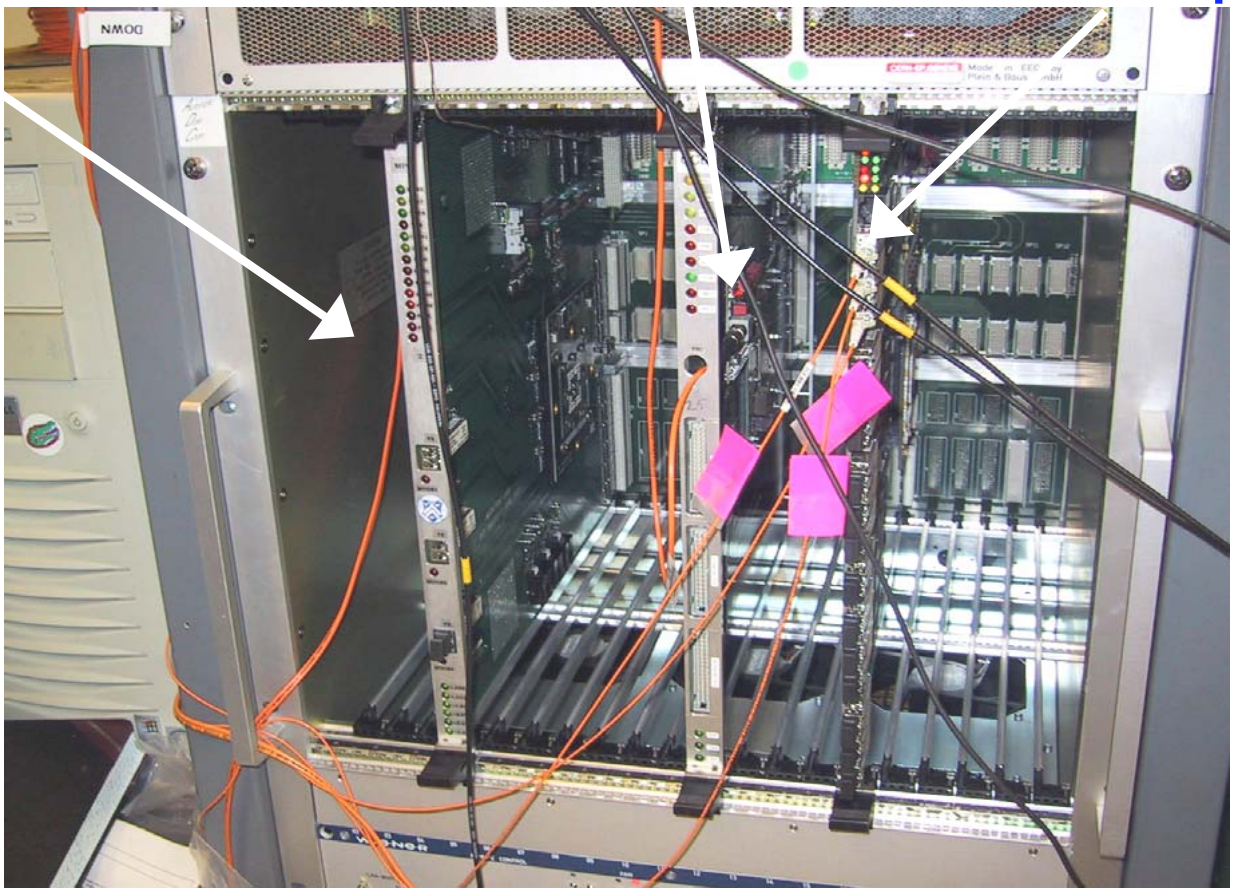
CSC Track-Finder Crate

Florida

MPC, for in-crate tests

CCB with TTCRx

Sector Processor, receives optical data



Second generation prototypes tested at beam test

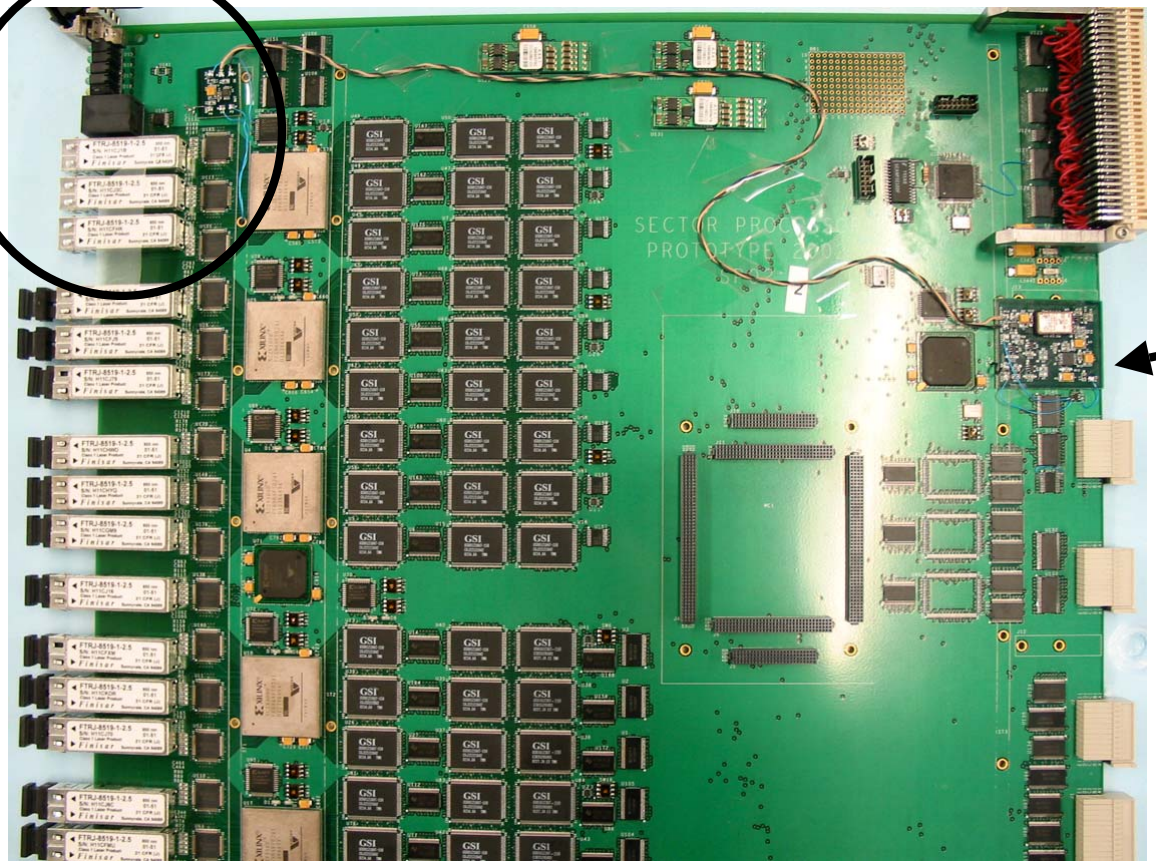
CSC Track-Finder (SP) Trigger

Florida

Test 3 x 1.6 Gb/s optical link connections from CSC electronics

Uses TLK2501 chipset from TI

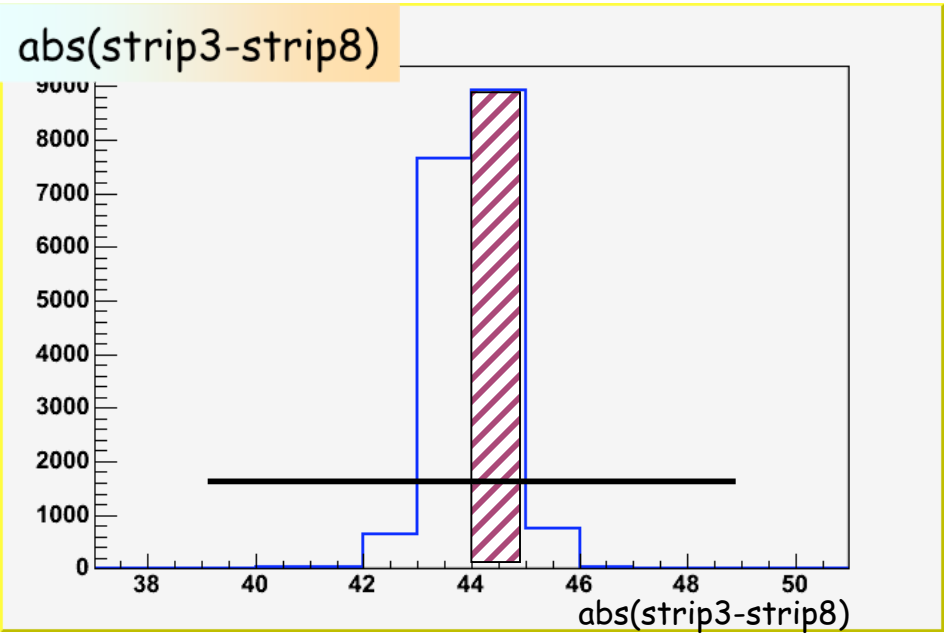
Home-built VCXO & PLL clock patch added to clean incoming TTC clock for links, but TTC QPLL also tested

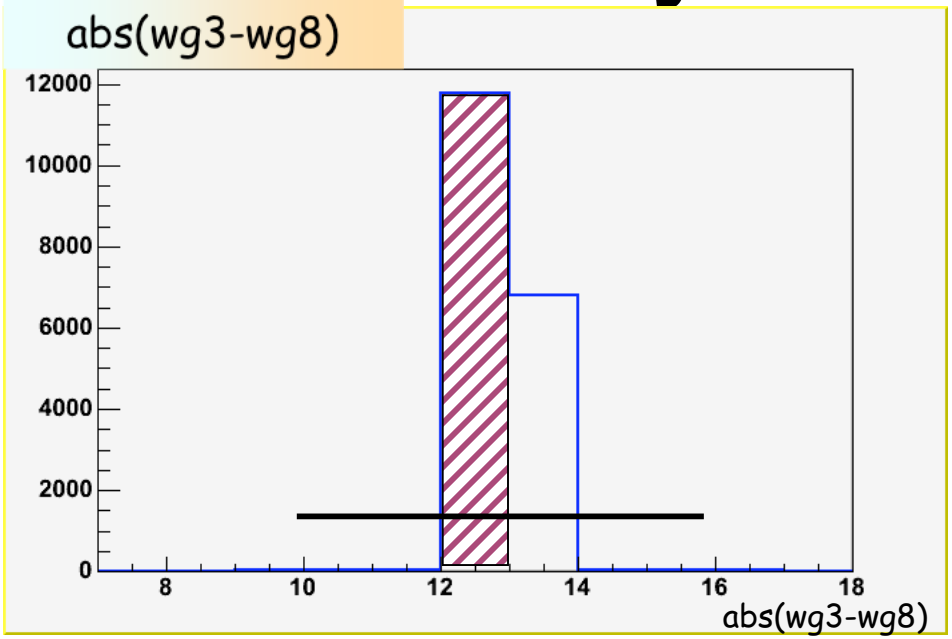


Requires very stable reference clock for error-free operation

Errors during May tests without PLL

Structured Beam Tests Correlated LCT Efficiency





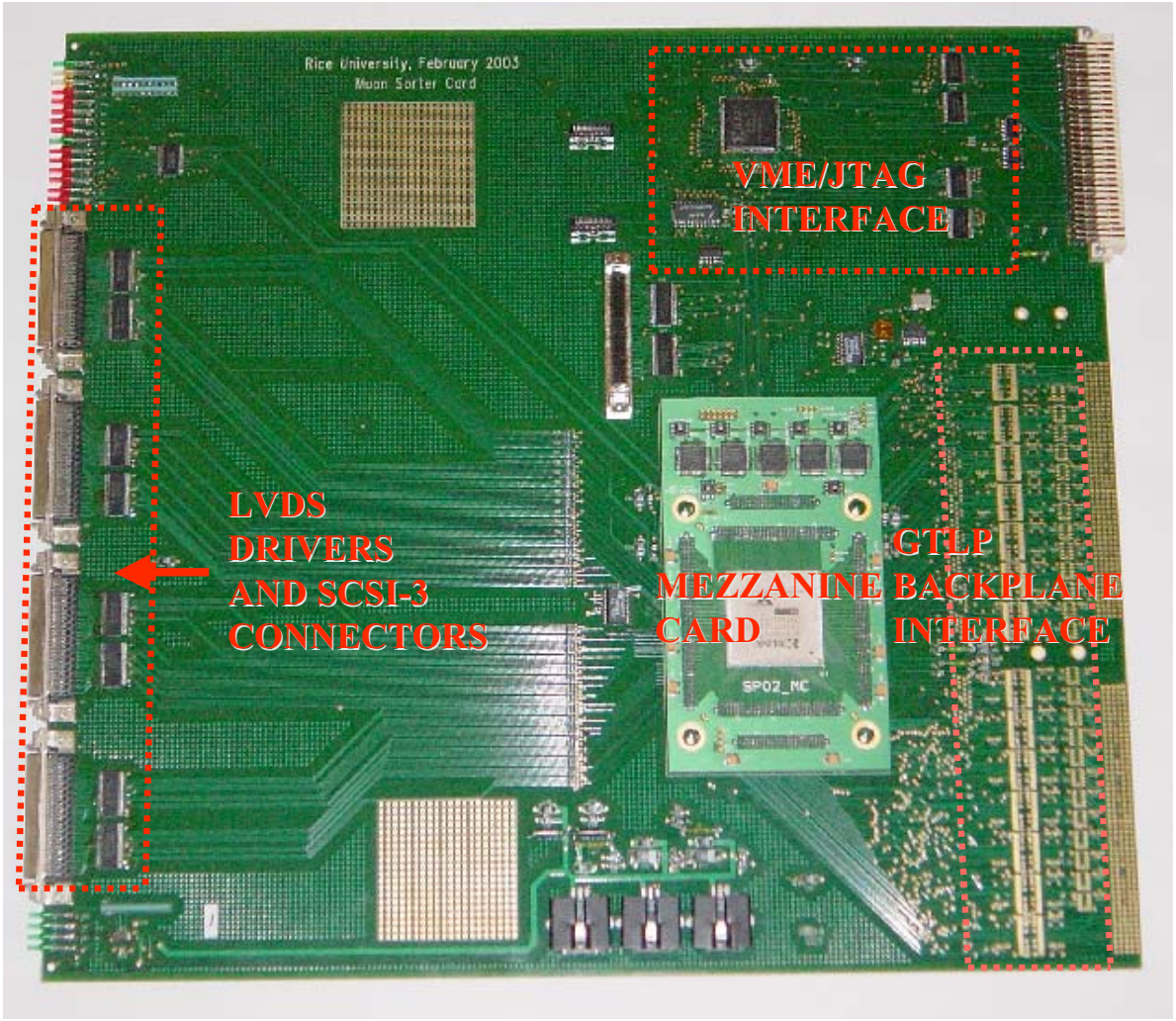
The efficiency to identify a correlated LCT (ALCT+CLCT) in one csc in a straight-line path from an LCT found in the other csc (within a ±5 strip and ±3 WG tolerance) is:

- 97.9% in one BX
- 98.9% in two BX (correct BX or one after)
- 99.1% in three BX (correct BX ±1)

as determined from logged Track-Finder data

Muon Sorter

Rice



Have 4 boards in hand, all stuffed (except front panel connectors to GMT)

Have dedicated Wiener 9U crate with VME J1 backplane and custom Track Finder backplane installed

Sector Processor – to – MS interface test currently underway

CSC Trigger Status/Plans

Muon Port Card, Clock Control Board, Sorter mostly validated

- Waiting for further integration tests before production
- CCB design revision to incorporate new CERN Clocking

CSC beam test with Track-Finder was a success!

- Complete electronic chain test of synchronous data transmission from CSC front-end electronics to the Track-Finder
- Latest Clocking System from CERN tested and works

Initial tests show that DT and CSC Track-Finders can exchange data

- Minor interface problems are trivial to address.

Remaining CSC Trigger tests underway

- Some delay, but production should complete in early 2005